

JEDEC STANDARD

Radio Front End-Baseband (RF-BB) Interface

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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RADIO FRONT END-BASEBAND (RF-BB) INTERFACE

Foreword

This standard establishes the requirements for an interface between Radio Front End (RF) and Baseband (BB) integrated circuits (IC). These requirements are intended to ensure that multiple RF and baseband IC vendors can collaborate and design a common IC interface allowing each of the devices to work with each other. Included are requirements for electrical signaling, link layer state machines and register map definitions.

Introduction

This interface is a high-speed, low latency digital interface that has been defined primarily for wireless local area networking applications but can be used for other RF to BB links such as used in metro area networking and wide area networking applications. This interface allows the radio front end of a wireless network controller to be separated from the base-band and MAC device(s) by up to 50 cm. A typical example is to connect a radio front end in the upper (screen) portion of a laptop computer to a base-band device on the motherboard. Lower power options are also defined for shorter distances.

The basic interface consists of three differential signals totaling to six pins. A clock signal must be provided by the FED on one pair of pins along with two pairs of pins for data transfers from the FED to BED and in the reverse direction. A separate pair is dedicated for either direction. Figure 1 illustrates the pin connections for the RF-BB interface. An optional pair of pins can be assigned for a return clock from the BED to the FED.

The interface provides three, concurrent, logical channels for communication: a streaming data channel, a control channel and a register access channel. Each of these channels can be programmed by the BED, subject to the constraints indicated by the FED in its capability registers. The FED determines the clock frequency, while the BED can select the data frame formats subject to the constraints indicated by the FED in its capability registers. Registers defined in clause 7 control the streaming rate, data and control word sizes, and optional configurations.

I.1 Features

- 1) Flexible interface usable for multiple standards
- 2) Low power duty cycle data and clock sub-modes
- 3) Low analog complexity
- 4) Low latency data transfer configurable down to 20 ns¹
- 5) Raw link bandwidth of up to 2.3 Gb/s depending on clocking speed
- 6) Double data rate (DDR) clocking
- 7) Rejects 30 dB of interference with the use of differential signaling
- 8) Low radiated emissions from differential signaling
- 9) Clocking frequency (up to 1.1GHz) under the control of FED
- 10) Supports 0-50 cm line lengths

¹ Streaming-data latency is affected by the number and word bit length of the streaming words in one RF-BB interface frame. Fewer streaming words and smaller word bit lengths will result in lower latency, but will also lower the bandwidth efficiency of the interface. If bandwidth is abundant, then the latency can be configured to be around 20 ns.

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RADIO FRONT END–BASEBAND (RF-BB) INTERFACE

(From JEDEC Board Ballot JCB-05-105, formulated under the cognizance of the JC-61 Committee on Wireless Interface Network.)

1 Scope

The normative information in this standard is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to this specification. Additional informative information is provided in the appendices to help illustrate the normative material.

This document addresses the following interface topics:

- 1) RF-BB Electrical layer: time and amplitude specifications for lines, drivers, receivers, clocks;
- 2) RF-BB Link layer: bits, clock-data synchronization, power modes;
- 3) RF-BB Transport layer: data types, data framing, data bandwidth, connection to core IC;
- 4) RF-BB Interface Registers.

This document defines a high-speed serial link that enables the bi-directional transfer of data and control information between the FED and BED. The document does not mandate the use of specific signaling, standard framing or standard messaging needed to make this an interoperable interface standard for RF devices or BB devices.

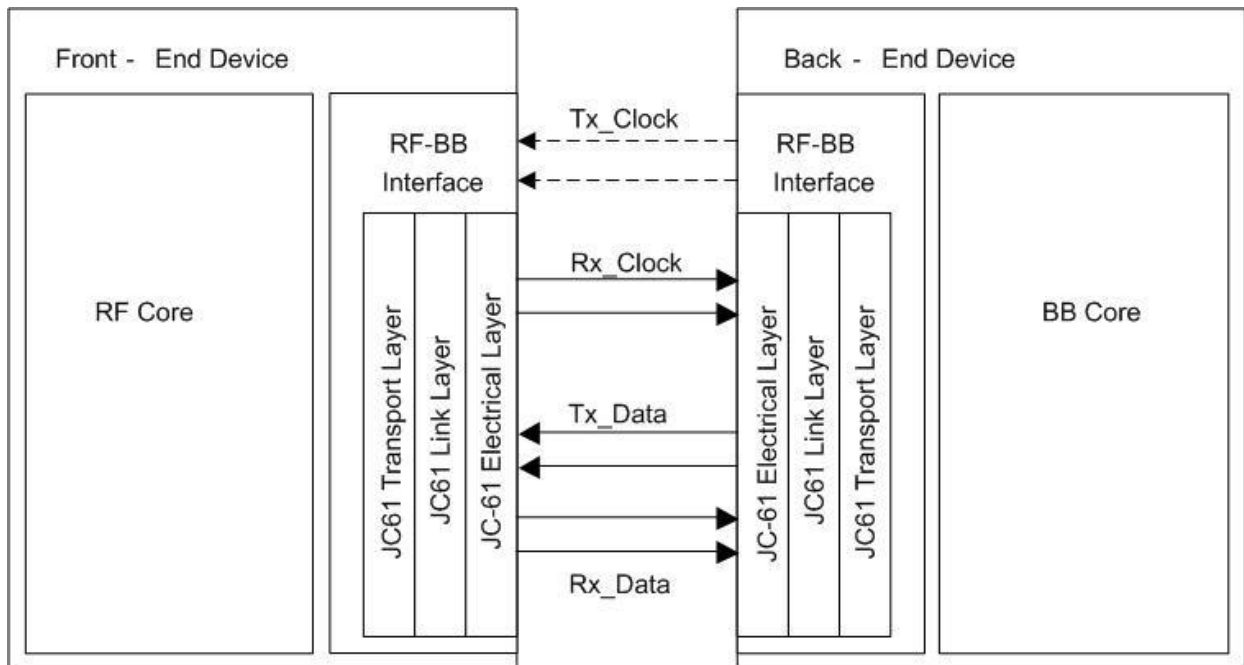


Figure 1 — Interface layer diagram

Specific implementations of this interface are beyond the scope of this standard.

2 References

2.1 Informative

The following standards contain provisions that, through references in the text, are informative in this standard. At the time of publication, the editions indicated were valid. All standards are subject to revisions.

IEEE Std 802.11-1999, *Wireless Local Area Network (WLAN) Standards*, (Reaffirmed 2003)

TIA/EIA-644-A, *Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits*, February 2001.

JESD8-13, *Scalable Low-Voltage Signaling for 400 mV (SLVS-400)*, October 2001.

High Speed Serialized AT Attachment rev. 1.0; 29 August 2001 Specification.

HyperTransport™ I/O Link Specification Revision 1.03.

2.2 Normative

JEP106M, *Standard Manufacture's Identification Code*, May 2003

3 Terminology

For the purpose of this standard, the following terms, definitions, acronyms and abbreviations apply.

3.1 Terms and definitions

base-band frequencies: Low frequencies neighboring and including 0 Hz. These frequencies are represented with real In-Phase (I) and Quadrature (Q) parts or together as a complex signal. In this document, the word “base-band” will usually refer to a base-band processor (part of the BED in this interface).

common mode voltage: The average voltage level of the two signals on a differential line.

deskew: The act of aligning a clock with incoming data so that the clock edge can be used to latch data in the middle of the data eye.

frame: A group of serial bits consisting of a Sync Mark, Header, and one or more of the following fields:
1) streaming data, 2) control data, 3) register data, and 4) parity bit.

radio: A device or a group of devices that translates the information bandwidth between base-band and the radio frequency portion of the spectrum.

Rx-direction: Direction of Receiving from Front End Device to Back End Device.

Rx-link: Data link that moves data from Front End Device to Back End Device.

TX-direction: Direction of transmitting from the Back End Device to the Front End Device.

TX-link: Data link that moves data from Back End Device to Front End Device.

little endian: The format in which the least significant bit (LSB) of a word is transferred first and the most significant bit is transferred last.

3 Terminology (cont'd)

3.1 Terms and definitions (cont'd)

big endian: The format in which the most significant bit (MSB) of a word is transferred first and the least significant bit is transferred last.

TX_IN: Single-ended combination of TX/TXN analog signals received by FED.

TX_DATA_VALID (FED): Indication the TX_IN signal contains data for the FED Transport Layer.

TX_CLK: Clock signal from FED Link Layer to the FED Transport Layer that has been deskewed for maximum data eye opening on TX_IN.

RX_OUT: Single-ended serial data from the FED Transport Layer to the FED Link Layer which is synchronized with CLK_90.

RX_DATA_VALID (FED): Indication that the RX_OUT signal contains data for the FED Link layer.

CLK_90: 90-degree-offset clock signal provided by the FED Link Layer to the FED Transport layer to synchronize outgoing RX_OUT.

LINK_REQUEST: Indication that the Transport layer requires FED Link Layer services. This could also serve as a data clock request.

DESKEW_REQUEST: Indication that the Transport layer needs the Link to deskew incoming data and clocks. One possible reason to send this is because of some CRC error seen in the Transport layer.

LINK_STATUS: This signal reports that the Link is ready, or not ready. It is related to DESKEW_STATUS as well.

TX_CM_DET: Indication to the FED Link layer from the FED Electrical layer that a minimum active common mode voltage has been detected on the TX/TXN lines.

RX_EN: Enables the RX/RXN drivers on the FED Electrical Layer to transmit.

CLK_0 (FED): FED: Single-ended zero-phase-offset clock from the FED Link layer for the CLK/CLKN driver in the FED Electrical Layer.

CLK_0 (BED): BED: Single-ended clock signal from the BED Electrical Layer to the BED Link Layer corresponding to CLK/CLKN.

CLK_EN: Enables the CLK/CLKN drivers on the FED Electrical Layer to transmit.

CLK_DET: Indication to the BED Link layer that the BED Electrical Layer has detected a minimum active common mode voltage on the CLK/CLKN lines.

RX_CM_DET: Indication from the BED Electrical layer to the BED Link Layer that a minimum common mode voltage was detected on the RX/RXN lines.

RX_IN: Single-ended analog BED signal corresponding to the received differential RX/RXN signal in the BED Electrical Layer.

TX_EN: Enables the TX/TXN drivers in the BED Electrical layer to transmit.

TX_OUT: Single-ended data to be driven differentially on TX/TXN.

3 Terminology (cont'd)

3.1 Terms and definitions (cont'd)

TX_DATA_VALID (BED): Indication from the BED Transport Layer that TX_OUT contains valid data for the BED Link Layer.

RX_DATA_VALID (BED): Indication that signals from the BED Link layer on RX_IN contains data for the BED Transport Layer.

3.2 Acronyms and abbreviations

| | |
|---------------------|-------------------------------------------------------------------------------------------------------------------------|
| BED | Back-end device. Relative to the RF-BB interface, the BED is the baseband processor. |
| BW | Bandwidth |
| CLK, CLKN | The Clock differential pair |
| DDR | Double data rate clocking. Data clocked on both the rising and falling edges of the interface clock signal. |
| Def | Default Value |
| FED | Front-end device. Relative to the RF-BB interface, the FED is the radio frequency device. |
| Flight Delay | Propagation time of the signal on a transmission line |
| HDR | Header |
| MAC | Medium access Control |
| PHY | A Wireless LAN, MAN or PAN physical layer interface . The bottom layer of the JC-61 RF-BB is called “electrical layer”. |
| RF | Relating to a Radio Frequency device. |
| RF-BB | Relating to the interface between a Radio Frequency device and a Baseband processor. |
| Rx | Receive |
| RX, RXN | The Receive differential pair signals |
| TX, TXN | The Transmit differential pair signals |
| Tr | Rising or falling transition time. The time it takes to transition from one defined signal level to another. |
| Tx | Transmit |
| UI | Unit interval or bit interval. For double data rate clocking, the unit interval is half of a clock cycle. |
| VCM | Common mode voltage. |

3 Terminology (cont'd)

3.2 Acronyms and abbreviations (cont'd)

WLAN Wireless data packet network in a general sense, including IEEE 802.11, wireless Metropolitan Area Networks, including IEEE 802.16; and wireless Personal Area Networks, including IEEE 802.15.

3.3 Numeric representation

The numerical values are in decimal unless indicated otherwise. The values specified in decimal are coded in natural binary unless otherwise stated.

4 Electrical layer

The JC-61 physical data link is designed to deliver a scalable level of bandwidth and interconnect distance performance between a Front-End IC (FED) and a Back-End IC (BED) using a robust LVDS signaling variant similar to HyperTransport™.

The physical layer can operate in one of four power modes – which are distinguished by different transmission impedance levels. The high power mode utilizes a standard differential source and load termination impedance of 100 Ω . This mode enables data links with transmission rates up to 2.3 Gb/s per data pair and up to a maximum distance of 50 cm at full rate.

The three low-power modes utilize higher transmission impedance to save driver power. These modes utilize nominal differential termination impedances of 200 Ω or 300 Ω , or high impedance, and are restricted for use with shorter interconnect distances and lower rates as listed in Table 3. For the third power mode, the interface is operated with asymmetric termination impedances utilizing a 100 Ω (differential) source impedance of the driver together with high impedance termination at the receiver. Due to the high amount of reflection possible in this type of line interface, only lower data rates can be supported. Power consumption is reduced in the asymmetric termination mode for lower data rates.

It is required to use one of the termination impedance modes. An optional device impedance discovery process is also available for switching to low power modes. At power-up the termination on the FED and BED can be decided a priori or both the devices can power-up in the 100 Ω mode and then switch modes via register access.

4.1 Electrical layer overview

The basic I/O interface consists of three differential signals that utilize a total of 6-pins on each device. Figure 2 illustrates a typical RF-BB interface with DDR clock sourced from FED to BED. Synchronous serial NRZ data links are provided in both directions between FED and BED. . An optional pair of pins can be assigned for a return clock from the BED to the FED.

The RF-BB interface is distinguished from other LVDS serial interfaces by its ability to signal in either direction a wake-up signal to a receiver side that is powered off – by using the power enable in the driver to raise the common mode voltage level at the line receiver input. When powered off, the driver will pull down the differential termination voltages to ground. When powered on, the driver will raise the common mode voltage of the termination to specified levels. This capability allows the implementer of an attached device to manage the power dissipation in the interface and system so that the total power is minimized when the interface and/or system components are not in active use.

4 Electrical layer (cont'd)

4.1 Electrical layer overview (cont'd)

The RF-BB interface standard also provides the option for Clock and Data duty-cycling modes where the Data drivers and Clock driver may be powered down between frames. The fast common mode signaling capability (i.e., Duty-cycling modes) of this interface may be used to conserve additional power when full data link bandwidth is not needed.

For example, in an RF-BB link configuration, when the (RF) FED is powered off, the base-band (BED) may power up the FED oscillator and interface by common mode signaling on the Tx Data link pins.

Similarly, when the interface is powered off in the RF (FED) and base-band (BED) devices, the FED may signal a power-on request by common mode signaling on the Clock pins.

The I/O data bandwidth is scalable to rates greater than 2.3 Gb/s by adding additional data-link pairs in the direction desired (see 5.7). Any additional data-link pairs operate synchronously using the single common source clock. Power management of an expanded data interface is accomplished the same way by using common mode signaling between the designated driver and receiver.

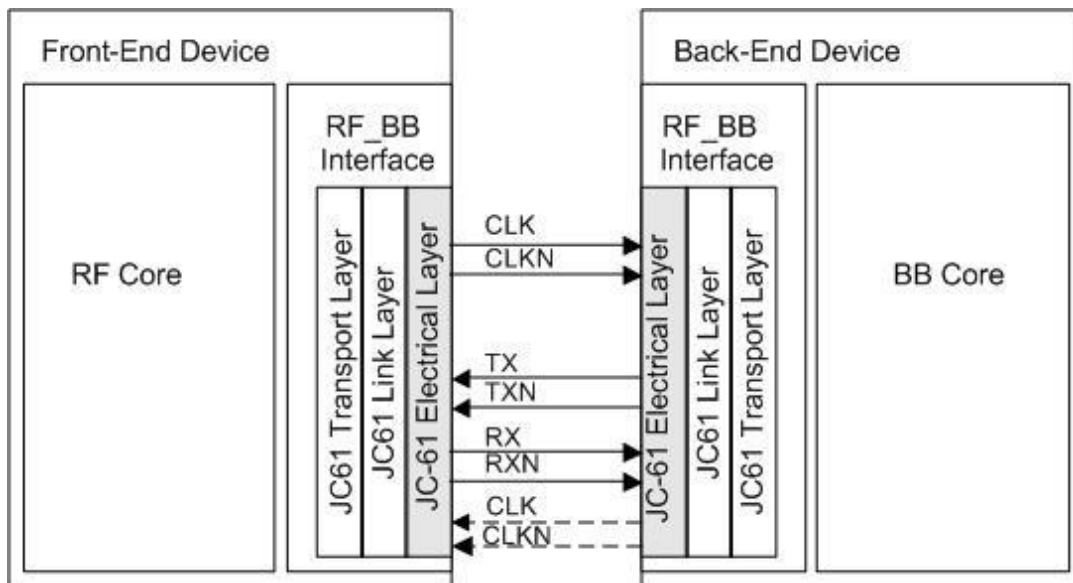


Figure 2 — Electrical Layer Connections

4.1.1 Common mode rise-time and detection delays

For the situation where duty-cycled power management options are not used, only the maximum total common-mode signal detection time is specified. Otherwise where duty-cycled power management options are used, the common mode activation rise-time and detection time delays are specified to be shorter than the maximum total common mode activation delay, in order to realize improved average power efficiency.

The Common Mode Activation Delay is defined as the total time required between the logic activation of the common mode power-up at the I/O driver cell to the detection of the common mode signal present at the I/O receiver cell logic.

4 Electrical layer (cont'd)

4.1.1 Common mode rise-time and detection delays (cont'd)

Maximum Common Mode Activation Delay shall be 100 ns, except when the optional duty-cycled modes are used.

In order to support low-overhead duty-cycled modes, the suggested driver maximum CMV rise time (20% to 80%) is 1 ns. The Common Mode Activation Delay time for these modes is required to be less than 10 ns.

4.1.2 Common mode noise

The RF-BB interface shall be designed to operate with Common Mode Noise levels between the driver and receiver of up to 200 mV p-p, including common mode DC offsets of up to 100 mV dc. The common mode noise may be anywhere in a bandwidth of DC to 200 MHz.

4.2 Power supply characteristics (informative)

The I/O supply is a single fixed supply with nominal VIO assumed to be in the range of +1.2 vdc to +3.3 vdc, excluding supply tolerance. Different supply voltages may be used for FED and BED devices with assurance that they will be compatible at the interface. Power supply characteristics provided in table 1 are for guidelines purposes only.

Table 1 — Link power supply characteristics

| Parameter | Description | Min | Typ | Max | Units |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------|-----|-------|
| VIO Nominal | Range of nominal I/O supply voltages supported for RF or BB devices | 1.2 | | 3.3 | V |
| VIO Tolerance | Supply DC Tolerance | -10 | | +10 | % |
| Supply Noise (External) | AC ripple noise peaks, DC to 10 MHz | -50 | | +50 | mV |
| Typical driver current per pair* | 100 Ω termination mode – High Power Mode 200 Ω termination mode – Low Power Mode 1 300 Ω termination mode – Low Power Mode 2 | | 6.0 3.0 2.0 | | mA |
| Typical receiver current per pair* | | | 1.0 | | mA |
| * These typical currents are not requirements; they are informative only and will depend on specific implementation details, including the current requirements of input/output pads and other supporting circuits. | | | | | |

It is recommended that the RF-BB interface specifications support driver and receiver designs that consume zero supply current when in the sleep state.

4.3 Driver cell DC specifications

The DC specifications of the driver are valid and should be measured only when the circuitry has assumed steady-state conditions.

Figure 3 gives a reference circuit that can be used in ATE verification testing or simulations. The reference circuit utilizes ideal balanced DC termination resistance. Note that for drivers that support the low-power transmission options, it will be necessary to test with the optional higher impedance reference loads indicated in Table 2.

4 Electrical layer (cont'd)

4.3 Driver cell DC specifications (cont'd)

The DC specifications below apply directly at the transmitter output pins DO+ and DO-, and ensure that the driver circuits are adequately balanced and provide correct source impedance and correct differential and common mode output levels, from a DC perspective.

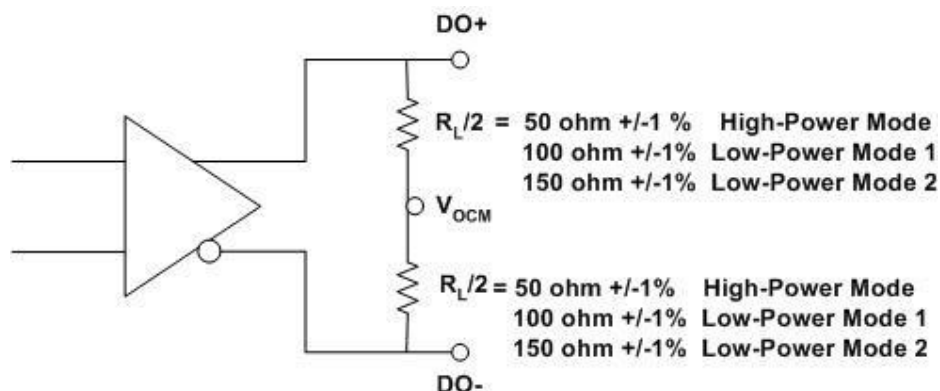


Figure 3 — DC Output reference system load

Table 2 — Driver DC Specifications

| Parameter | Description | Min | Typ | Max | Units |
|----------------------------------------|--------------------------------------------------------------------------------------------|-------|------|-------|----------|
| Source resistance (each output leg) | High-power mode, Low-power mode 3 | 45 | 50 | 55 | Ω |
| | Low-power mode 1 | 90 | 100 | 110 | |
| | Low-power mode 2 | 112.5 | 150 | 187.5 | |
| | Low-Power mode 3 (High Z) | 37.5 | 50 | 62.5 | |
| V_{OD} | Peak Differential output voltage ¹ - terminated $V_{OD} = DO+ - DO- $ modes | 470 | 600 | 755 | mv |
| | Low-power mode 2 | 400 | 600 | 900 | |
| | Low-power mode 3 | | 1200 | | |
| Change in V_{OD} | Change between logic "1" and "0" states | -20 | | +20 | mv |
| V_{OCM} average | $(V_{OCM}^{11} + V_{OCM}^{00}) / 2$ | | | | mv |
| | High Power, Low power mode 1 | 495 | 600 | 715 | |
| | Low power modes 2, 3 | 450 | | 800 | |
| Change in V_{OCM} | Change between logic "1" and "0" states | -20 | | +20 | mv |
| Output impedance match | Absolute difference between logic "1" and logic "0" state output impedances | 0 | | 5 | % |

NOTE DC voltage specifications assume on-chip resistance calibration to +/-10% or better.

4.4 Driver cell AC specifications

These parameters place requirements on the driver under idealized load and add dynamic signal characteristics of the driver caused by signal transitions at the intended operating frequency and power supply limits. Since the specification supports a wide range of speed grades and interconnect/impedance options, the reference load and associated specifications are broken down into a number of "corner" limit cases that have specific recommended reference load circuits for ATE verification or simulation.

For all corner cases, the driver signal parameters associated are measured at the termination side of an idealized transmission line load relative to the average common mode voltage level at the termination.

4 Electrical layer (cont'd)

4.4 Driver cell AC specifications (cont'd)

Table 3 — AC reference system load characteristics

| Case | Description | R_L | Max Clock Rate (MHz) | Line Length (cm) | Z_0 (Ω) | Line to Line Time Skew | C_L (pf) |
|------|---------------------------------------------|-------|----------------------|---------------------------|----------------------|------------------------|------------|
| 1. | High-speed Long-length High-power | 100 | 1150 | 50 | 50 (loss 1.2 dB) | <15 ps | 2.0 |
| 2. | Med-speed Long-length High-power | 100 | 600 | 100 | 50 (loss 1.5 dB) | <30 ps | 4.0 |
| 3. | Med-speed Med-length Low-power 1 | 200 | 600 | 10 (PCB trace length) | 100 (loss 0.3 dB) | <30 ps | 2.0 |
| 4. | Med-speed Low-power 2 | 300 | 300 | 3.0 (PCB trace length) | 130 nom. | <50 ps | 2.2 |
| 5. | Low-speed Low-power 3 (100 Ω) | Hi-Z | 200 | 5.0 | 50 | <50 ps | 4.0 |

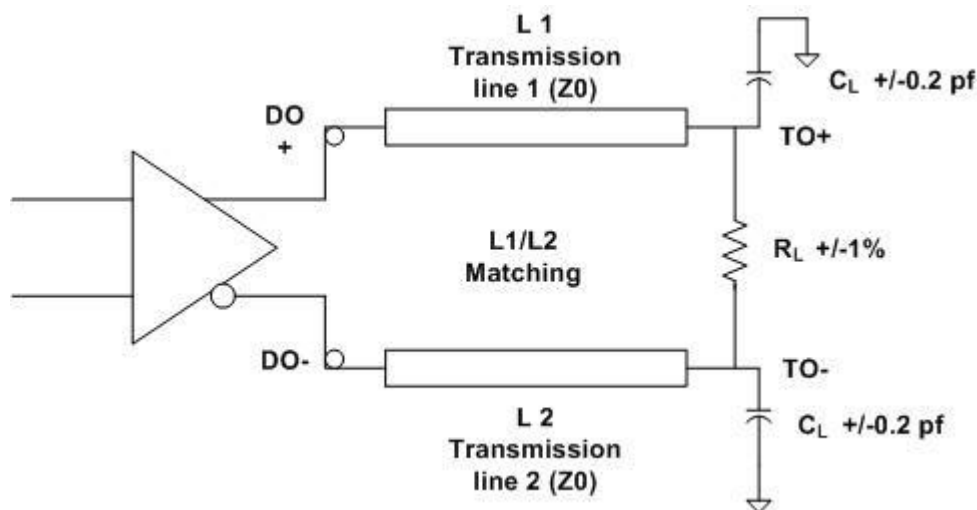


Figure 4 — AC reference system load

The AC reference system constitutes an ideal matched and balanced load, with appropriate skew tolerance on the complementary transmission lines. The characteristic line impedances (Z_0) of L1 and L2 for cases 1 and 2 shall be matched to within $\pm 2\%$.

For shorter interconnect distances, such as in cases 3, 4, and 5, the interconnections are likely to be controlled impedance traces on a PCB or module substrate. For these cases, the AC reference line impedance should be controlled to $\pm 10\%$ with matching of $\pm 5\%$ or better.

For case 4, the line is short enough to be considered a lumped trace capacitance. In this case, the combined driver output capacitance and receiver input capacitance is specified to be 4 pf maximum. Line impedance of 130 Ω $\pm 15\%$ shall be utilized for the reference load system.

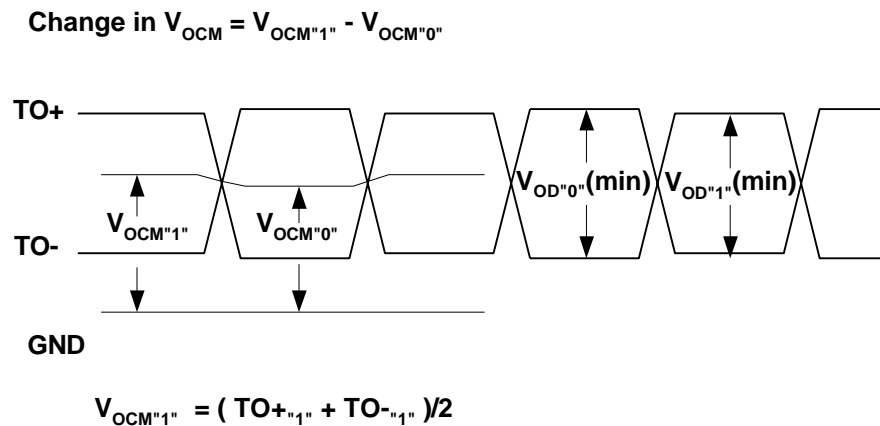
4 Electrical layer (cont'd)

4.4 Driver cell AC specifications (cont'd)

The five “corner” cases above are used within clause 4. These were selected to represent safe upper capability limits of speed, line type, and loading for RF-BB applications of practical interest. AC and timing specifications are given for these corner cases, with the understanding that some relaxation of specifications are possible for ranges between these corner case limits. The capacitive loading represents a model of typical IC + PCB pad node capacitance and may be exceeded in some implementations. Similarly, actual line lengths may exceed those in Table 3. For those cases, de-rated speed performance levels should be determined with appropriate design simulations. Suggested interconnect line specification limits for RF-BB interface designs corresponding to these corner cases are given in 4.6.1 and include wider tolerances than those called out here for the driver AC reference load circuits.

4.4.1 AC signal level parameters

AC signal level parameters are measured at designated clock speed at the end of the reference system transmission line at each terminal, TO+ and TO-, with respect to ground. The common mode voltage is an average of the complementary load voltages at TO+ and TO- for each logic state, as indicated in Figure 5. Since the waveform may have overshoot and undershoot due to impedance mismatches, the differential output signal level is measured with respect to the minimum points in the settled state of the waveform, as indicated.

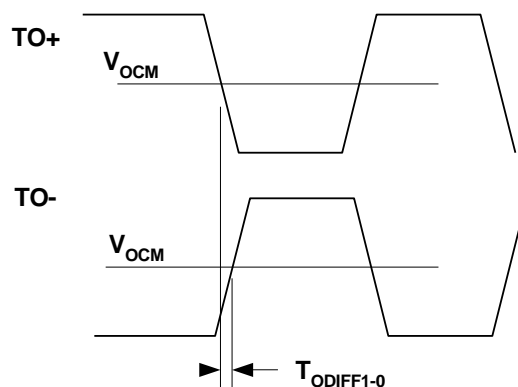


NOTE These parameters measure the effects of AC impedance imbalances, and non-linearity when coupled to an appropriately balanced and loaded line.

Figure 5 — Driver AC waveform parameters

4.4 Driver cell AC specifications (cont'd)

4.4.1 AC signal level program (cont'd)



$$T_{ODIFF} = (T_{ODIFF1-0} + T_{ODIFF0-1})/2$$

NOTE The parameter T_{ODIFF} defines the allowable differential skew as measured in a single-ended fashion at the average V_{OCM} level (midpoint) of the transition of the true signal and complement signal at the termination. It is the average difference for both logic 0-1 and 1-0 transitions.

Figure 6 — Differential output skew

4.4.2 Driver AC specifications

The specifications in Table 4 are broken down relative to the speed capabilities and corner case loading assumptions defined in Table 3.

Table 4 — AC specifications

| Parameter | Description | Min | Typ | Max | Units |
|------------------------------|-------------------------------------------------------------------------------------------------------|--------------------------|-----|---------------------------|-------|
| Output L (each leg) | IC output inductance with IC package | | | 4.0 | nH |
| Output C (each leg) | IC output pad capacitance with IC package Cases 1, 3, 4 Case 2, 5 | | | 1.8 3.0 | pF |
| V_{OD} | Ave. (min.) peak differential voltage at termination Cases 1. & 2 Case 3. Case 4. Case 5. | 250 350 250 | | 650 750 800 1300 | mV |
| V_{OD} change | Change between “1” and “0” states | -75 | | 75 | mV |
| V_{OCM} | Ave. output common mode voltage High Power, Low Power Mode 1 Low Power Modes 1 & 2 | 400 250 | | 800 800 | mV |
| V_{OCM} change | Change between “1” and “0” states | -50 | | 50 | mV |
| Rising and falling edge rate | Between +/-50 mV points on differential signal Case 1. Case 2. Case 3. & 4 Case 5. | 2.5 1.5 1.0 1.0 | | 8.0 6.0 4.0 5.0 | V/ns |
| Edge rate matching | Mismatch of rise and fall rates | | | 5 | % |
| T_{ODIFF} | Midpoint skew between “+” and “-” output signals Cases 1. & 3. Case 2. & 5. Case 4. | | | 35 70 100 | ps |

4.5 Receiver cell specifications

4.5.1 Receiver DC specifications

The DC specifications below apply directly at the receiver input pins RI+ and RI-, and ensure that the receiver operates statically over a range exceeding the worst case input signal range of a RF-BB link. The receiver may have on-chip termination resistor, off-chip resistor, or a combination of these. The reference circuit below assumes that the differential termination is internal.

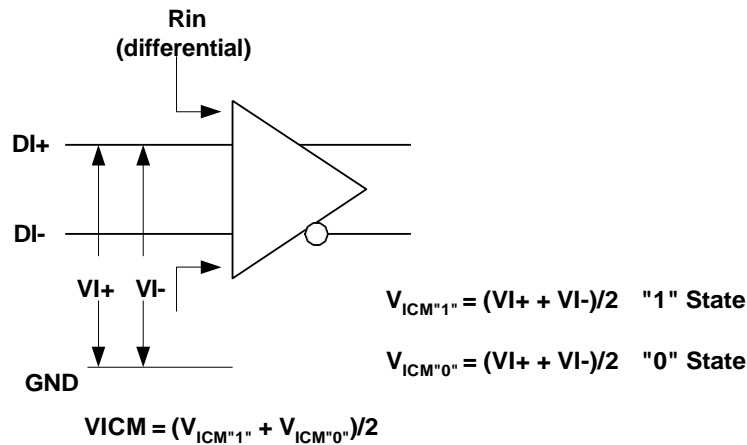


Figure 7 — Receiver reference circuit

Table 5 — Receiver DC specifications

| Parameter | Description | Min | Typ | Max | Units |
|---------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|--------------------------|-------------------|-------------------|----------|
| Differential input resistance | High-power mode Low-power mode 1 Low-power mode 2 Low-power mode 3 | 90 180 225 1000 | 100 200 300 | 110 220 375 | Ω |
| Input voltages, VI+, VI- | Maximum allowable safe DC range at input terminal DI+ or DI- | -200 | | 1200 | mV |
| Differential input voltage | Peak magnitude $ (V_{I+} - V_{I-}) $ allowable, consistent with V _{ICM} and max safe limits | 200 | | 1300 | mV |
| Change in diff. input voltage | Difference in amplitude from logic "1" to "0" state allowable in input signal | -100 | | 100 | mV |
| Input common mode voltage, V _{ICM} | Allowed V _{ICM} = (V _{I+} + V _{I-})/2 High Power, Low Power mode 1 Low power modes 2,3 | 360 200 | 600 | 860 900 | mV |

4.5.2 Receiver AC specifications

These parameters place requirements on the receiver, and are derived from the output parameters of the drivers and various interconnect characteristics. They include a parameter that defines the presence of common mode noise in a system between driver and receiver.

Input termination AC impedance specifications are provided and shall include the impedance tolerances for all configurations of external and on-chip terminations.

4.5 Receiver cell specification (cont'd)

4.5.2 Receiver AC specification (cont'd)

For receiver testing or simulation modeling, the device should be driven by an ideal driver through ideal interconnect such as described in Table 3 and Figure 4 according to the input parameters defined herein. The load capacitance shown in Figure 4 represents the input capacitance of the receiver and input trace.

Table 6 — Receiver AC Specifications

| Parameter | Description | Min | Typ | Max | Units |
|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|--------------------------|-------------------|--------------------------|----------|
| Input inductance, each leg | IC pad and package impedance | | | 4.0 | nH |
| Input capacitance, each leg | IC pad and package impedance Cases 1, 3, 4 Case 2, 5 | | | 1.8 3.0 | pF |
| Differential input impedance (mid-band) | High-power mode Low-power mode 1 Low-power mode 2 Low-power mode 3 (Hi-Z) | 90 180 225 1000 | 100 200 300 | 110 220 375 | Ω |
| Input Common Mode Voltage, V_{ICM} | Extremes including “0” and “1” states with CM noise - High Power Mode and Low Power Mode 1 Low Power Mode 2 & Mode 3 | 360 200 | | 860 900 | mV |
| Common Mode Noise | Peaks relative to V_{ICM} DC average | -100 | | 100 | mV |
| Differential input signal level, V_{ID} | Peak magnitude, including signal fidelity distortions Terminated modes Low-power mode 3 – Hi-Z | 200 400 | | 850 1300 | mV |
| Differential Edge Rate (-50 mv to 50 mv) | Cases 1. Cases 2. Case 3. & 4. Case 5. | 2.0 1.5 0.5 1.0 | | 8.0 5.0 2.0 5.0 | V/ns |
| Edge rate matching | Absolute difference of rise and fall edge rates | | | 5 | % |

4.6 Interconnect specifications

The interconnect specifications are recommended limits for interconnect parameters that are consistent with the corner cases defined in 4.4 for different combinations of upper data rate, distance, and interface impedance mode. These are suggested specifications based on simulations that will ensure link robustness with the timing parameters specified in 4.7. Connectors may be used, provided that the interconnect, including the connectors, meet the specified parameter limits for the relevant case(s).

4.6.1 Line specifications

The interconnect line specifications below correspond to the corner length and speed cases in 4.4. Interconnect schemes operating outside of these limits should be verified by simulation to meet receiver and link timing requirements.

4.6 Interconnect specifications (cont'd)

4.6.1 Line specifications (cont'd)

Table 7 — Suggested corner case interconnect specifications

| Case/Parameter | Description | Min | Typ | Max | Units |
|-------------------------------|--------------------------------------------------------------------|-----|------------|-----|----------|
| Case 1 | 50 Ω lines (up to 2.3 Gbps) | | | | |
| Length | Length of specification | | 50 | | cm |
| Z_0 | Single-ended mode Differential mode | 45 | 50 60 | 55 | Ω |
| Z_0 Matching | (line to line) | | | 2 | % |
| DCR | Resistance at DC (each line) | | | 3 | Ω |
| Time skew | (line to line) | | | 15 | ps |
| HF attenuation | Loss at 1150 MHz | | | 1.2 | dB |
| Crosstalk | (pair to pair) | | | -26 | dB |
| Eye amplitude closure | Ideal +/-10% terminations Amplitude closure relative to average | | | 25 | % |
| Case 2, Case 1 except: | 50 Ω lines (up to 1.2 Gbps) | | | | |
| Length | Length of specification | | 100 | | cm |
| Z_0 | Single-ended mode Differential mode | 45 | 50 60 | 55 | Ω |
| Z_0 Matching | | | | 5 | % |
| DCR | (each line) | | | 6 | Ω |
| Time skew | (line to line) | | | 40 | ps |
| HF attenuation | Loss at 600 MHz | | | 1.5 | dB |
| Case 3, Case 2 except: | 100 Ω lines (up to 1.2 Gbps) | | | | |
| Z_0 | Single-ended mode Differential mode | 80 | 100 120 | 120 | Ω |
| Length | | | 10 | | cm |
| DCR | (each line) | | | 2 | Ω |
| Time skew | (line to line) | | | 40 | ps |
| HF attenuation | Loss at 600 MHz | | | 0.3 | dB |
| Case 4 Case 1 except: | 130 Ω lines (up to 800 Mbps) | | | | |
| Length | | | 3.0 | | cm |
| Z_0 | Nominal trace layout impedance (minimize mismatch capacitance) | 110 | | 150 | Ω |
| Z_0 Matching | (line to line) | | | 5 | % |
| DCR | (each conductor) | | | 1 | Ω |
| Time skew | | | | 30 | ps |
| Total IO capacitance | (total driver, receiver IO capacitance, each node) | | | 4.0 | pf |
| HF attenuation | RC attenuation at 400 MHz | | | 2.0 | dB |
| Capacitance matching | Difference in total node capacitances | | | 5 | % |
| Eye amplitude closure | Ideal +/-10% terminations | | | 40 | % |
| Case 5 Case 2 except | 50 Ω lines (up to 400 Mbps) | | | | |
| Length | | | 5 | | cm |
| DCR | | | | 2 | Ω |
| Time Skew | | | | 80 | ps |
| Eye amplitude closure | Hi-Z output termination | | | 40 | % |

4.7 Physical layer I/O timing requirements

Similar to the HyperTransport™ link, the RF-BB data link from FED to BED uses source-synchronous clocked transfers for transmit and receive frames across the interconnect. Transfer timing is dependent upon the driver devices outputs, the interconnect medium, and the receiver device's input timing characteristics to control the time skew induced between clock and data signal edges. The amount of skew, signal fidelity distortion, timing alignment uncertainty, required receiver set-up and hold window, and uncorrelated noise will jointly determine the data link frequency that can be attained reliably.

This specification uses a simple timing methodology that partitions the link-timing budget into four key parameters and accounts for simultaneous worst-case combinations of timing uncertainties due to edge skews, signal distortions, and noise. The BED or FED transmitter timing quality is specified by the signal characteristics at the termination end of an appropriate AC reference load that is ideally matched at the termination side. Zero-crossings of clock and data on matched lines define the total data-valid time interval within the bit period. The actual interconnect channel will introduce additional errors, based on the level, speed, reflections, and noise present in the signal at the line receivers. These factors are summarized in one timing jitter interval parameter that subtracts from the data-valid time that the receiver sees. The BED or FED receiver timing quality is specified by the minimum required data-valid width of the receiver input zero-crossings for reliable data recovery. The methodology is a pessimistic approach that attempts to cover all cases that are expected to occur in operational systems. Timing specifications are budgeted for each component (transmitter, interconnect channel, and receiver) and on the clock and data paths together in order to ensure a positive link margin when devices meet these specifications independently over process, voltage, and temperature corners. An example reference block diagram of the FED to BED data link is shown in Figure 8.

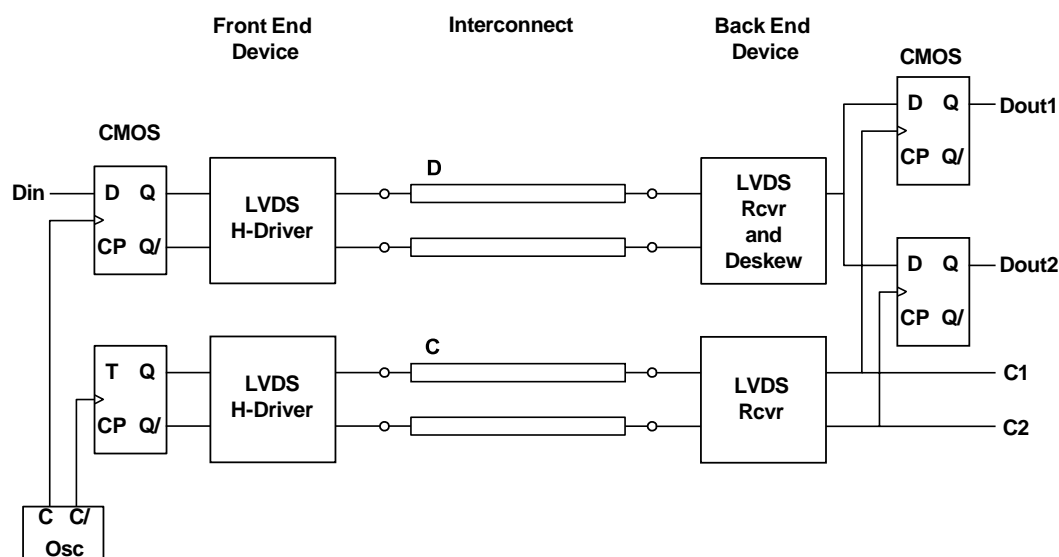


Figure 8 — Example block diagram of a FED to BED link

Timing parameters for the interface are defined relative to the Clock and Data signals at the receiver inputs, as illustrated by the eye diagram mask in Figure 9.

4.7 Physical layer I/O timing requirements (cont'd)

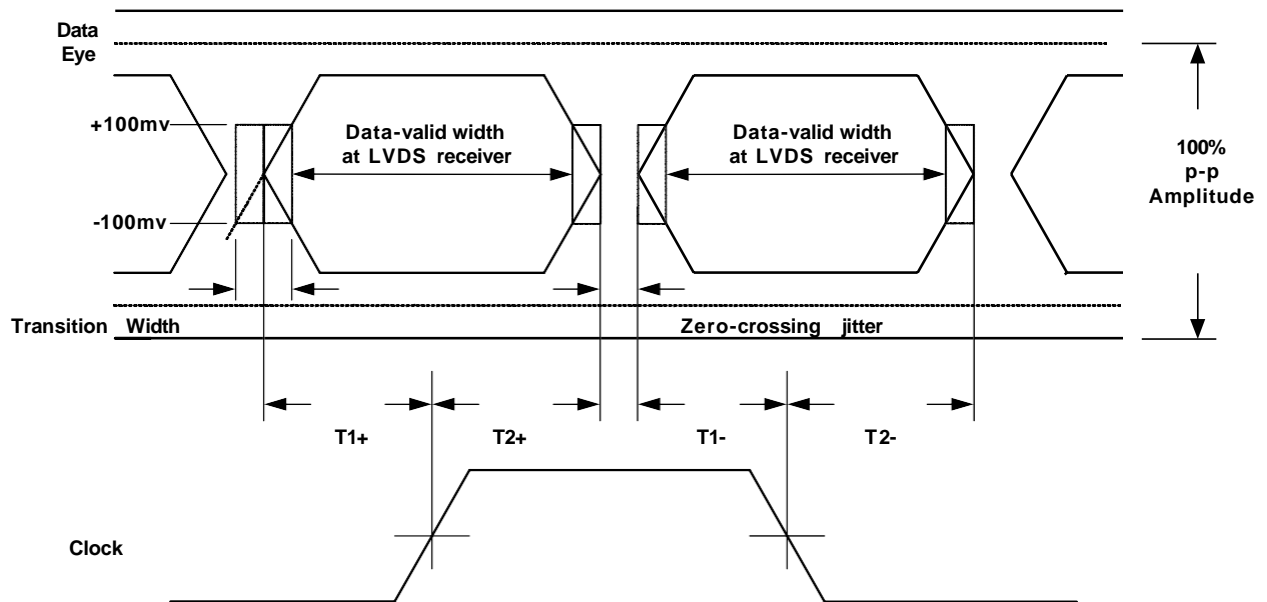


Figure 9 — Eye Diagram of data and clock at the receiver input

4.7.1 FED transmitter timing specifications

Transmitter timing quality is specified relative to the zero crossings of the differential signals at the end of ideal matched lines. For a DDR link, the Data edge skews relative to positive or negative Clock transitions and the transmitted Clock duty cycle errors define the available data valid windows at the receiver.

4.7.1.1 Phasing of clock and Rx data outputs

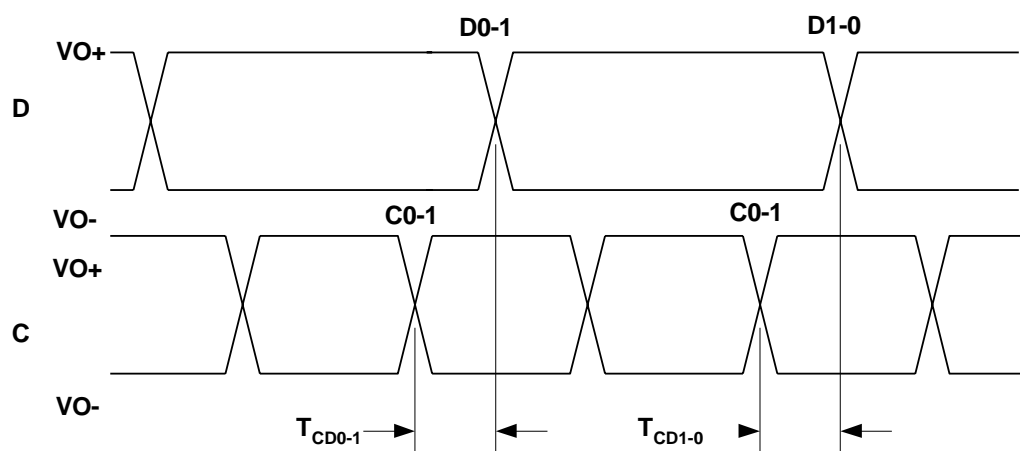
The clock and data outputs from the FED shall be nominally phased so that the clock edges are delayed by $90^\circ \pm 22.5^\circ$ of a clock period. This ensures that the DDR clock transitions occur near the mid-bit time and will limit the amount of timing deskew correction required in the BED receiver.

4.7.1.2 Phasing of clock and Tx data outputs

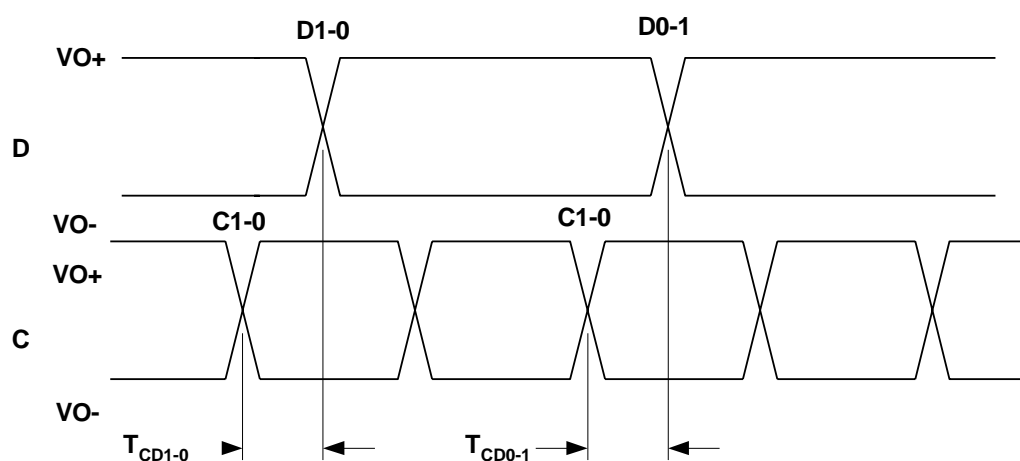
In the case of the usage of the optional return clock, the clock and data outputs from the BED shall be nominally phased so that the clock edges and data edges are aligned to be $90^\circ \pm 22.5^\circ$ apart.

4.7.1 FED transmitter timing specifications (cont'd)

4.7.1.2 Example - data and clock transition dependent skews



$$T_{C+D} = \text{ave} (T_{CD0-1}, T_{CD1-0}) \quad (\text{clock rise edge delay})$$



$$T_{C-D} = \text{ave} (T_{CD0-1}, T_{CD1-0}) \quad (\text{clock fall edge delay})$$

$$TCD_{DIFF} = | T_{C+D} - T_{C-D} |$$

NOTE The parameter TCD_{DIFF} is a measure of the average data-dependent skew jitter of the transmitted data edges. Relative to an ideal square source clock, this is the amount of time uncertainty that must be subtracted from a full data bit period due to jitter on the data stream.

Figure 10 — Data and Clock transition dependent skews

4.7.1 FED transmitter timing specifications (cont'd)

4.7.1.3 Example – clock duty cycle error

Similarly, the clock may have periodic edge jitter due to non-ideal duty cycle, as illustrated in Figure 11.

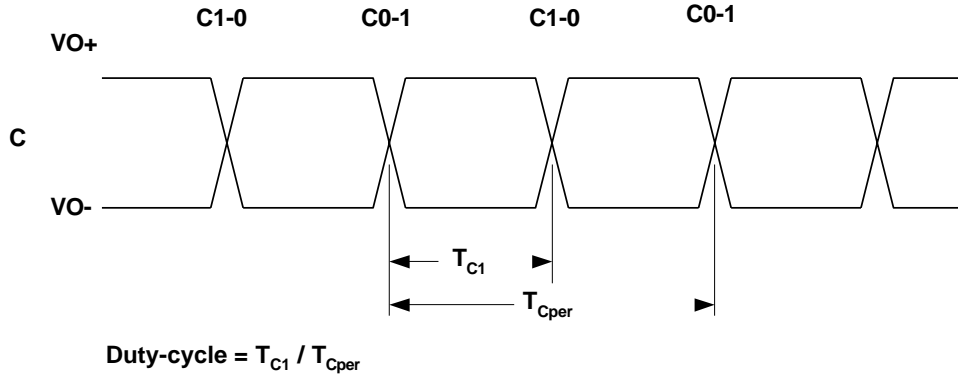


Figure 11 — Clock duty cycle error

The clock zero-crossing duty cycle shall be within 45% to 55%. Both types of timing errors subtract from the guaranteed data-valid window around each transmitted clock edge in a manner illustrated in Figure 11.

4.7.1.4 Transmitted data-valid window

At the receiver, the data-valid window available from the transmitter will be reduced by the clock edge variation due to non-square duty-cycle. The Transmit Data-valid Window, T_{DAV} is given in equation 1.

$$T_{DAV} = \min(T1+, T1-) + \min(T2+, T2-) \quad (1)$$

Where $T1+$, $T1-$, $T2+$, $T2-$ are defined in the eye diagram of Figure 9. This parameter does not depend on the absolute phase alignment of Data and Clock or the duty-cycle of the Clock directly, but does include the effects of duty-cycle, and data and clock transition skews that are illustrated in Figure 10 and Figure 11.

The data-valid window will be reduced at the line receiver due to the finite data transition width, as illustrated in Figure 9. The transition characteristics in the critical detection zone of the line receiver around the zero-crossings will depend on interconnect channel characteristics and I/O loading – the primary factors that cause the received edge rate to vary.

Thus the data transition width parameter is considered part of the interconnect channel timing error.

4.7.2 Interconnect timing error

The interconnection channel and line receiver will introduce significant additional timing errors at the receiver input due to finite data transition width, mismatch related signal distortion, and common mode noise that is not rejected by the receiver. For links that are not deskewed, the interconnect timing delay skew between clock and data pairs will also reduce the set-up and hold timing margins in the receiver.

Suggested guidelines for budgeting interconnect timing errors (excluding Clock-to-Data delay skew) for the typical corner cases defined in 4.4 are given in Table 8. Worst-case line mismatch conditions are assumed.

4.7 Physical layer I/O timing requirements (cont'd)

4.7.2 Interconnect timing error (cont'd)

Table 8 — Budgeted interconnect timing errors

| Corner case | Max data rate (Mb/s) | Typical edge rate (v/ns) | Data (+/-100mv) transition width (ps) | CM noise induced jitter 12-sigma (ps) | ISI time jitter p-p (ps) |
|-------------|----------------------|--------------------------|---------------------------------------|---------------------------------------|--------------------------|
| 1. HP | 2300 | 4.0 | 50 | 40 | 50 |
| 2. HP | 1200 | 2.5 | 80 | 65 | 100 |
| 3. LP1 | 1200 | 2.0 | 100 | 80 | 120 |
| 4. LP2 | 800 | 1.5 | 170 | 100 | 120 |
| 5. LP3 | 400 | 1.5 | 135 | 100 | 160 |

These time errors are additive, leading to the total interconnect channel timing error budgets in Table 9.

Table 9 — Corner case Interconnect Channel Timing Errors

| Corner Case | Max data rate (Mbps) | Total Interconnect channel timing error (ps) |
|---------------|----------------------|----------------------------------------------|
| 1. HP, 50 cm | 2300 Mbps | 140 |
| 2. HP, 100 cm | 1200 Mbps | 245 |
| 3. LP1, 10 cm | 1200 Mbps | 300 |
| 4. LP2, 3 cm | 800 Mbps | 390 |
| 5. LP3, 5 cm | 400 Mbps | 395 |

The timing budgets should be considered guidelines only for the corner cases defined. Interconnect channel timing budgets should be verified by simulation for specific designs.

4.7.3 BED receiver timing specifications

The sampling flip-flops of the BED receiver require adequate set-up and hold times for reliable data reconstruction. The BED receiver will thus require the incoming data to be valid during a minimum time window around the incoming clock edge. In a manner similar to the transmitter data-valid window, the required minimum receiver data-valid window position may be different for each sense of the DDR clock edge.

The required receive data valid time then is the maximum of these two windows:

$$T_{RDV} = \max(T_{SU+}, T_{SU-}) + \max(T_{H+}, T_{H-}) \quad (2)$$

Where T_{SU+} and T_{H+} are associated with the rising Clock edge at the receiver input, and T_{SU-} and T_{H-} are associated with the falling Clock edge at the receiver input. These time intervals are defined with respect to ideal fast transition input signals at the line receiver inputs.

The required Rx data-valid window is independent of the Clock-to-Data alignment phase and the duty-cycle of the incoming clock. It represents the minimum time interval over which the incoming data bit must be stable for reliable receiver logic data reconstruction.

4.7 Physical layer I/O timing requirements (cont'd)

4.7.4 Link transfer timing specifications

The outbound Data from BED to FED is clocked from the reconstructed input clock received from the FED. Thus it is reasonable to require that the BED Tx data-valid window meet the same timing limit as for the FED Tx Data. Duty-cycle error contributions from the FED clock source will tend to propagate back from the BED since the same clock edges are used for return Data clocking. The amount of noise added in passing the clock to and from the BED is already accounted in the interconnect noise budget.

Table 10 defines suggested limits for link timing for both directions for the T_{DAV} and T_{RDV} timing parameters for clock rate ranges that increment in 200 MHz steps. Table 10 also suggests limits for residual data to clock timing error. These apply to transmit and receive window alignments whether a deskew mechanism is used or not in the receiver side, and include all factors of time alignment including the interconnect medium data to clock time skew.

The difference between MIN Tx Data-valid transmit window and the MAX required Valid window at the receiver plus residual window alignment error between data and clock phasing will define a worst case time interval available for all other errors associated with interconnect channel timing error. The remaining available budget for interconnect timing errors is also indicated in Table 10 for each clock frequency range.

Table 10 — Recommended link timing specifications

| Data rate limit Mbps/ UI, ps | Min Tx data- valid width (ps), T_{DAV} | Required Rx min. valid width, (Max – ps) T_{RDV} | Max residual data to clock align error (ps) | Max available for interconnect channel error (ps, p-p) |
|---------------------------------|------------------------------------------------|----------------------------------------------------------|---------------------------------------------------|--------------------------------------------------------------|
| 2300/ 435 | 370 | 200 | +/-15 | 140 |
| 1600/ 625 | 520 | 240 | +/-25 | 230 |
| 1200/ 833 | 630 | 280 | +/-25 | 300 |
| 1000/ 1000 | 780 | 320 | +/-50 | 360 |
| 800/ 1250 | 1000 | 360 | +/-100 | 440 |
| 600/ 1667 | 1320 | 440 | +/-200 | 480 |
| 400/ 2500 | 2100 | 560 | +/-400 | 640 |

These timing specifications apply at the upper end of the clock ranges indicated. If actual clock frequencies are below the upper limits, it will be possible to increase the amount of time available for residual data to clock alignment error and interconnect channel timing errors.

This specification methodology assumes pessimistic adding of worst-case errors in each part of the data link. The total available data-valid time from the transmitter has been budgeted with no provision for excess margin. Specific design cases that fall outside of the limits or are close to the limits should be verified with appropriate simulations.

5 Link layer

The Link Layer provides bit communications services and functions to the Transport Layer and requires the services and functions of the Electrical Layer. The primary function for the Link layer is to establish and provide a channel for communicating bits. To this end, the layer maintains synchronization between data and clocking signals so that bits are clocked at the point of maximum eye-diagram opening. This layer is also where sleep and link states of the interface are established.

5.1 Link service

Figure illustrates the various components associated with the transport, link and electrical layers for the FED and BED. These generic signals are not necessarily comprehensive or sufficient, but are meant to be illustrative of the kinds of signals passed between the layers. These signals are defined in 3.1

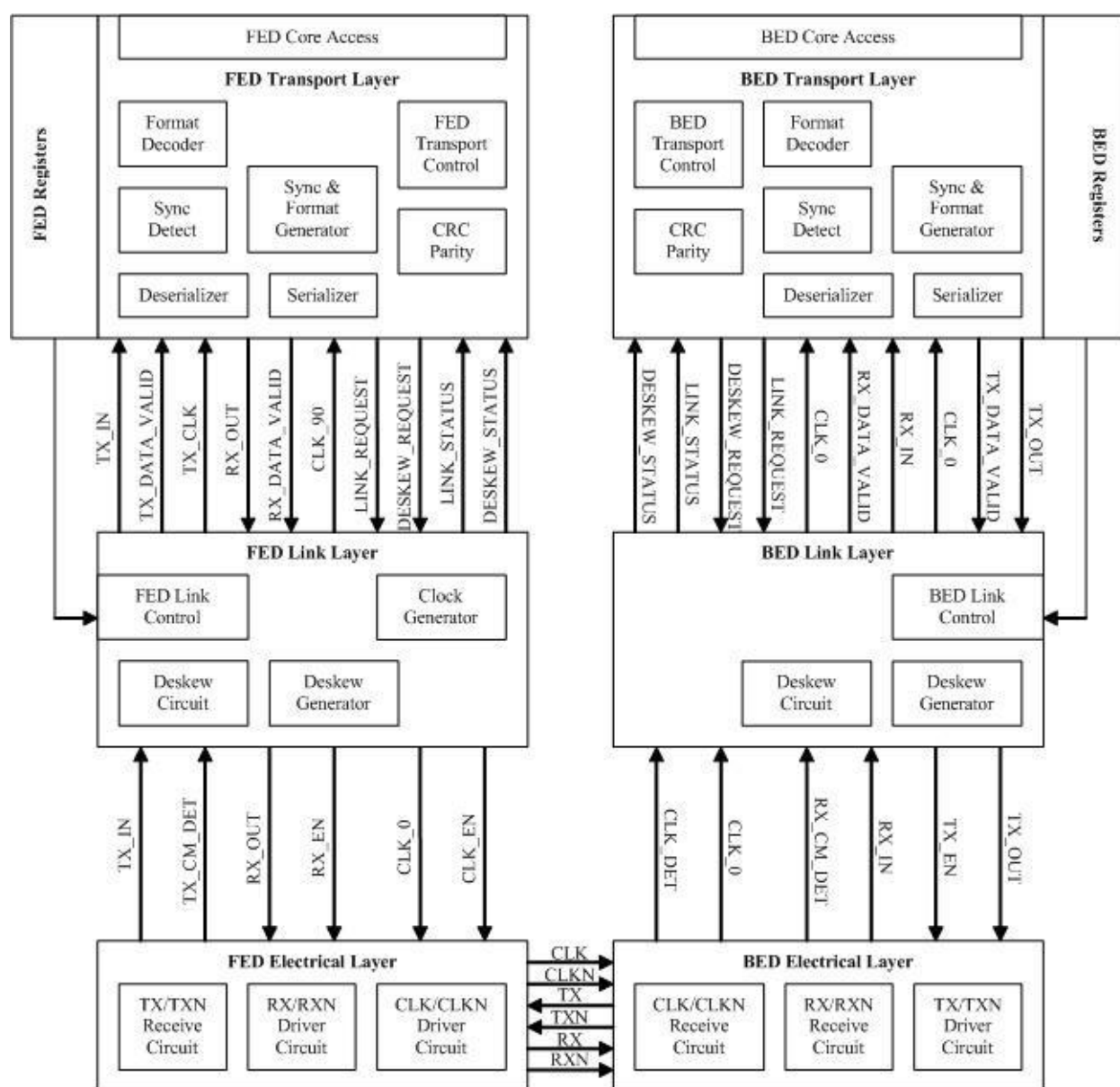
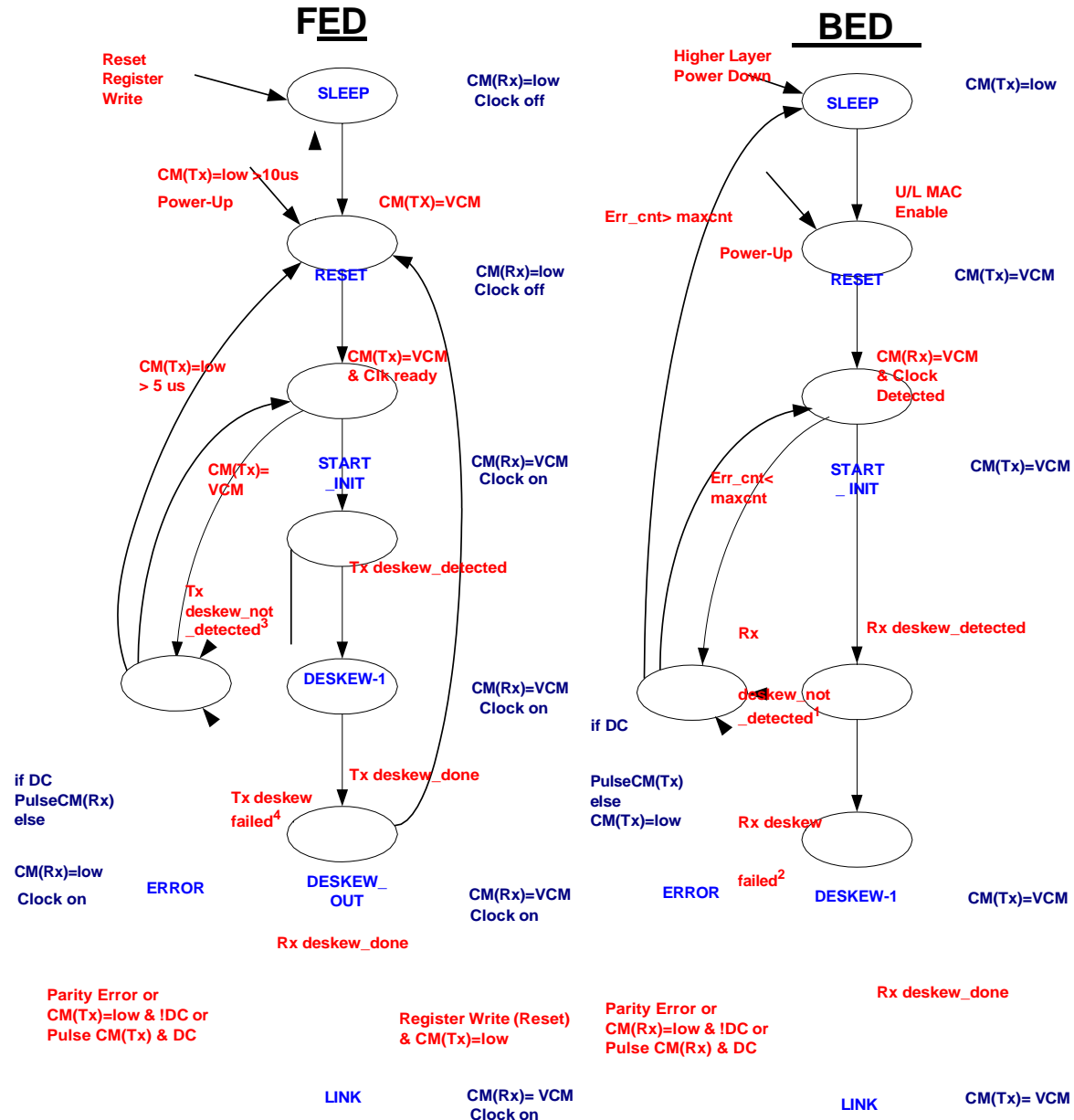


Figure 12 — JC-61 Link Layer and adjacent layers

5 Link layer (cont'd)

5.2 Initialization state diagram

To establish the service functions, the Link Layer must first undergo initialization. Initialization is automatic upon power up of either interface device.



¹ Rx_deskew detect is active if a deskew signal is detected on the RX/RXN pins and the deskew counter value is less than 2048; if not then the Rx_deskew_not_detected goes active; Rx_deskew_not_detected also goes active if CM(Rx) is not present and BED transitions to the error state.

² Rx_deskew_done is active if the BED completes the deskew process and the counter value is less than 2048; if not then the Rx_deskew_failed goes active. The Rx_deskew_failed can go active if CM(Rx) is not present and the BED transitions to the error state.

³ Tx_deskew detect is active if a deskew signal is detected on the TX/TXN pins and the deskew counter value is less than 128; if not then the Tx_deskew_not_detected goes active. The Tx_deskew_not_detected can also go active if CM(TX) is not present and the FED will transition into error state.

⁴ Tx_deskew_done is active if the FED completes the deskew process and the counter value is less than 2048; if not then the Tx_deskew_failed goes active. The Tx_deskew_failed can also go active if CM(TX) is not present and the FED will transition into error state.

Figure 13 — Link Layer initialization sequence

5 Link layer (cont'd)

5.2 Initialization state diagram (cont'd)

Upon power up or a higher layer Enable the BED will raise a common mode signal (CM(TX)=VCM) to notify the FED to wake-up. CM(TX) is considered to be low when both the differential signals, for example TX and TXN are at ground, and the differential mode of the signal is zero. Common mode on or common mode active (CM(TX)=VCM) implies taking the differential pair to a valid state with a common mode level at least equal to the minimum specified in clause 4. In the RESET State, the TX/TXN pins are driven to logic "1"; the FED starts the internal clock generator and both the FED and BED wait for the clock signal to be ready and stable on the CLK/CLKN pins. During the RESET state if the FED receives a common mode low on the TX pins for a duration greater than 10 us then the FED transitions into SLEEP state. Figure 14 illustrates the signal levels in the power-off and RESET States. The FED detects the common-mode signal on the TX lines. The TX/TXN common mode active also serves as a wake-up signal from the BED when the FED is in the SLEEP state.

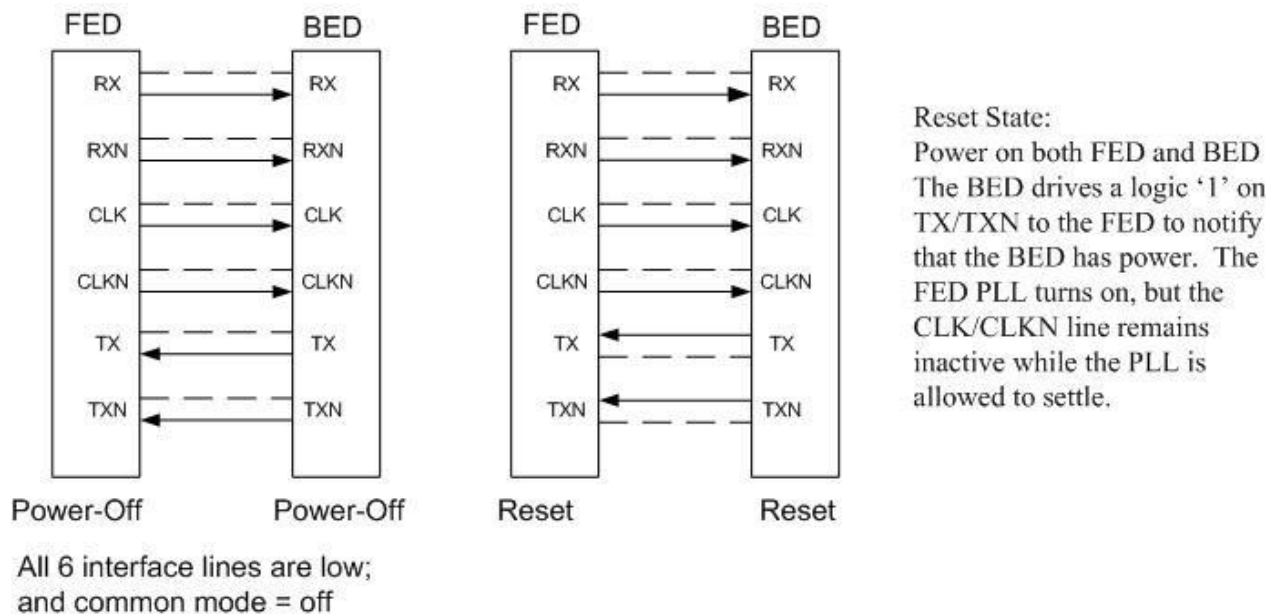


Figure 14 — Power-off and RESET states

Once the CLK signal is available and the BED detects CM(CLK)=VCM, the FED and BED transition into the START_INIT state. Figure 15 illustrates the signal levels when transitioning into the START_INIT state.

5 Link layer (cont'd)

5.2 Initialization state diagram (cont'd)

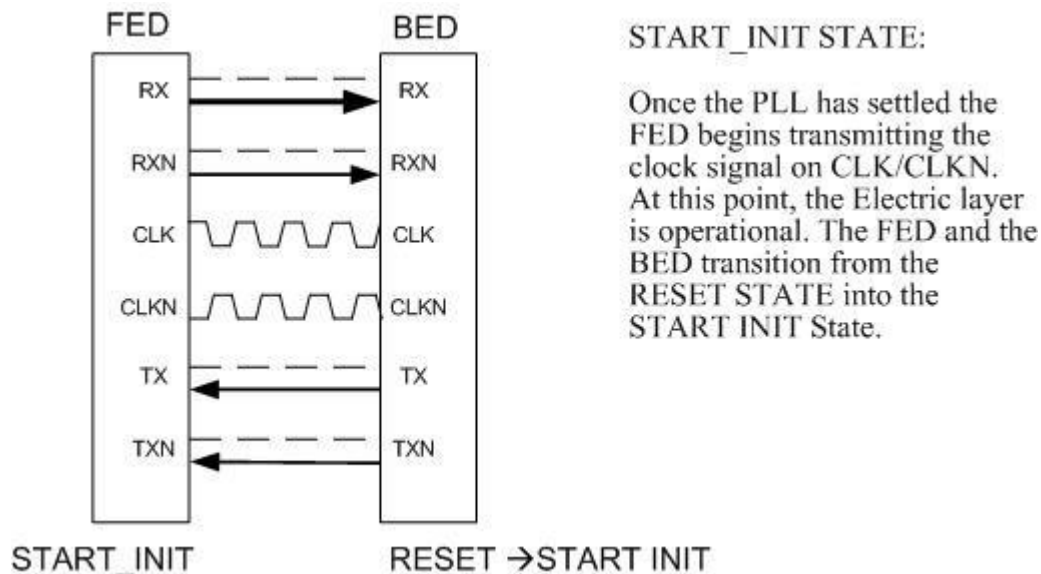


Figure 15 — START_INIT State

In the START_INIT state the BED starts to send out a deskew frame. The deskew frame consists of alternating 0s and 1s. The deskew process must complete within a maximum period of 2048 clock cycles, after which both the FED and the BED must finish deskew. The deskew process is deemed to be finished when the FED and/or the BED aligns the sampling clock signal at its most reliable instant i.e. center of the data eye opening. The deskew process does not have to take the 2048 clock cycles and can complete earlier. The method for aligning is implementation specific and is not discussed in this standard. The deskew counters on both the FED and BED start counting clock cycles once the clock signal is valid.

Deskew Pattern: 01010101 ... 01010101

The FED detects the deskew signal on pins TX/TXN and transitions into the DESKEW1 state. The FED performs a deskewing operation on the incoming TX signal using an internal clock or if available the return clock from the BED. The deskewing operation aligns the TX input data so that the clock samples the data at its most reliable instant, i.e., center of the data eye opening. On successful deskewing the FED transitions into the DESKEW_OUT state. During this state the FED sends out its own deskew signal on its RX output, indicating to the BED that the FED has successfully completed deskew. When the BED identifies the deskew signal at its RX input, the BED transitions from START_INIT state to the DESKEW-1 state. The BED stops its own deskew training signal and sets outputs to logic "1" and performs its own training and deskewing on the RX input. The signals are illustrated in Figure 16.

5 Link layer (cont'd)

5.2 Initialization state diagram (cont'd)

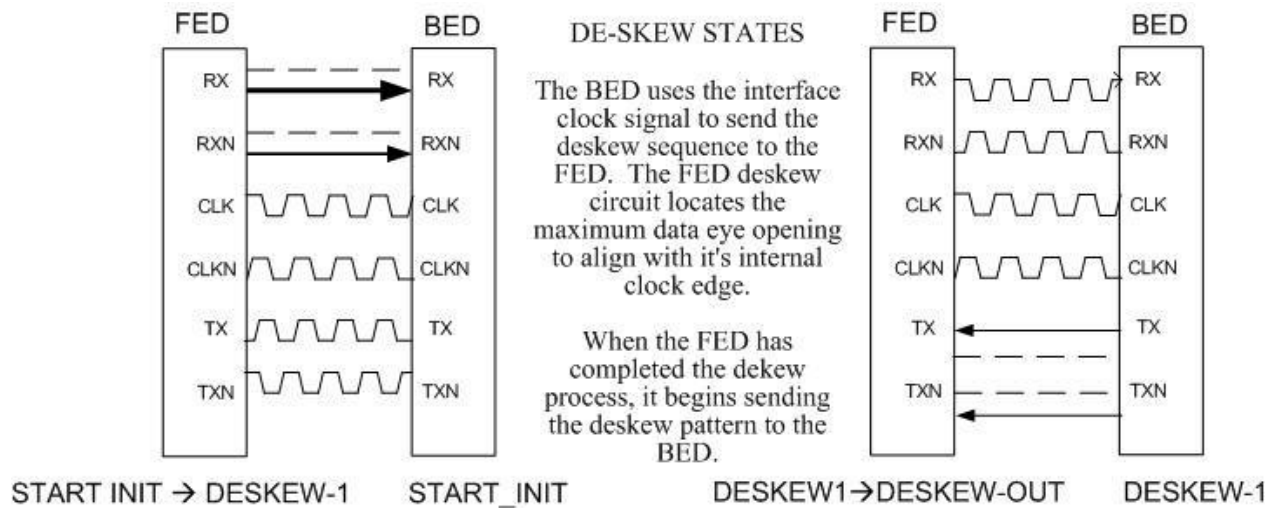


Figure 16 — DESKEW STATES

Once the deskew is complete on both sides the initialization is complete and the BED transitions into the LINK state. The FED, which was in the DESKEW_OUT state, transmits the training signal. The BED indicates the deskew process in progress by driving TX/TXN pin to logic high. On successful deskew, the BED drives the TX/TXN pin to logic '0' before moving directly into the LINK state. When both sides are in their specified LINK states, a successful link has been established and the RX/RXN and TX/TXN pins are in logic "0" state. The deskew process must complete in 2048 clock cycles once the clock signal has been established. It can also be completed in shorter time than the maximum allowed.

Figure 17 illustrates the signal levels during the link state. The link is now operational.

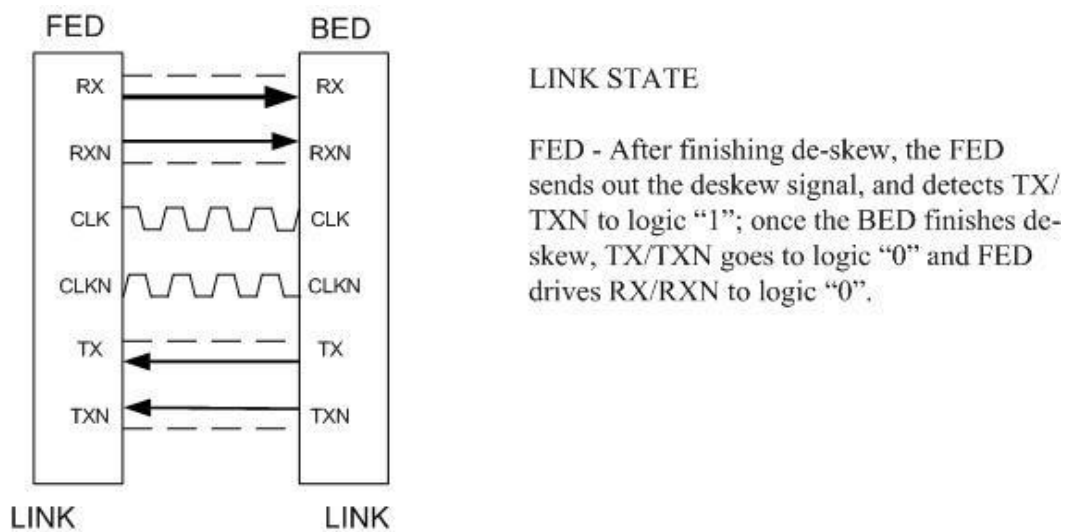


Figure 17 — LINK STATE

5 Link layer (cont'd)

5.2 Initialization state diagram (cont'd)

During the initialization process, there are several ways the sequence can breakdown and a device fail to establish a link. If the FED does not recognize the deskew signal after a period of 124 clock cycles after the establishment of a clock signal, a Tx_not_detected signal is generated and the FED transitions to the ERROR STATE. Also if the FED recognizes the deskew signal but is unable to successfully deskew before the deskew counter counts 2048 cycles, a Tx_deskew_failed signal transitions the FED to the ERROR STATE. In the ERROR STATE the FED drives the common mode to RX to low. The BED senses a common mode low and enters a ERROR state. The BED can also transition directly to the ERROR STATE by failing to detect the RX deskew signal or failing to successful deskew the RX deskew signal within the maximum deskew timeout of 2048 cycles. A maximum deskew timeout of 2048 cycles is provided for deskew of the FED and the BED separately, thus allowing a maximum of 4096 clock cycles for the deskew process.

In the ERROR STATE, the BED tallies the error count as either a FED failure or a BED failure and pulses the common mode of the TX output. This signals the FED to transition to the START_INIT. The initialization sequence begins again. As long as the maximum error count by either side is not reached, the BED continues to reset both sides and attempt initialization. If either side reaches a implementation defined maximum failure number, the BED transitions into the SLEEP STATE and the BED notifies the Station Management Entity within the MAC that a link cannot be established.

Table 11 and Table 12 summarize the state machine transitions. The operation during the LINK STATE and the transition from LINK STATE to the ERROR STATE is discussed in 5.6.1.

5 Link layer (cont'd)

5.2 Initialization state diagram (cont'd)

Table 11 — FED state machine transitions

| Current State | Next State | CM(Rx) | CLK | Transition Event |
|---------------|------------|---------------------------------------------------|-----|-------------------------------------------------------------------------------------------------------|
| SLEEP | | OFF | OFF | CM(TX)=OFF |
| | RESET | | | CM(TX)=ON |
| RESET | | OFF | OFF | Default state on Power-up |
| | START_INIT | | | CM(TX)=VCM & Clock Ready |
| | SLEEP | | | CM(TX)=OFF > 10usecs |
| START_INIT | | RX Logic “1” | ON | |
| | DESKEW-1 | | | Tx_deskew_detected* |
| | ERROR | | | Tx_deskew_not detected* or CM(TX)=OFF |
| DESKEW-1 | | RX Logic “1” | ON | |
| | DESKEW_OUT | | | Tx_deskew done† |
| | ERROR | | | Tx_deskew failed† or CM(TX)=OFF |
| DESKEW_OUT | | Deskew Signal | ON | |
| | LINK | | | TX transition from logic “1” to logic “0” |
| | ERROR | | | CM(TX)=OFF |
| LINK | | RX Logic “0” | ON | |
| | ERROR | | | Parity Error OR IF (Duty Cycle On) Pulse (CM(TX)) ELSE CM(TX)=OFF |
| | SLEEP | | | Write Mode Register |
| | RESET | | | Write Reset Registers & CM(TX)=OFF |
| ERROR | | IF (Duty Cycle On) Pulse (CM(Rx)) ELSE CM(Rx)=OFF | ON | State Machine will remain in ERROR state for at least 16 cycles before transitions out of ERROR State |
| | START_INIT | | | Tx(VCM)=OFF >5 usec; |
| | RESET | | | CM(TX)=OFF; |

* Tx_deskew detect is active if a deskew signal is detected on the TX/TXN pins and the deskew counter value is less than 128; if not then the Tx_deskew_not_detected goes active. Tx_deskew_not_detected also goes active if CM(TX) is not present and the FED transitions to the ERROR State. Deskew detection is not a separate function, but a condition reported after the deskew process (the search for optimum sampling phase) has already been started.

† Tx_deskew_done is active if the FED completes the deskew process and the counter value is less than 2048; if not then the Tx_deskew_failed goes active. Tx_deskew_failed also goes active if CM(TX) is not present and the FED transitions to the ERROR State.

5 Link layer (cont'd)

5.2 Initialization state diagram (cont'd)

Table 12 — BED state machine transitions

| Current State | Next State | CM(TX) | Transition Event |
|---------------|------------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| SLEEP | | CM(TX)=OFF | |
| | RESET | | Power-On & MAC enable |
| RESET | | TX Logic “1” | |
| | START_INIT | | CM(RX)=VCM & Clock Detected |
| START_INIT | | Deskew Signal | |
| | DESKEW-1 | | Rx_deskew_detected* |
| | ERROR | | Rx_deskew_not detected [†] OR CM(RX)=OFF |
| DESKEW-1 | | TX Logic “1” | |
| | LINK | | Rx_deskew done [†] |
| | ERROR | | Tx_deskew failed OR CM(RX)=OFF |
| LINK | | TX Logic “0” | |
| | ERROR | | Parity Error OR IF (Duty Cycle On) Pulse (CM(Rx)) else CM(Rx)=low |
| ERROR | | If (Duty Cycle On) Pulse (CM(TX)) else CM(TX)=low | State Machine will remain in ERROR state for at least 16 cycles before transitions out of ERROR State |
| | START_INIT | | Err_cnt < maxcnt; |
| | SLEEP | | Err_cnt >= maxcnt; |

* Rx_deskew detect is active if a deskew signal is detected on the RX/RXN pins and the deskew counter value is less than 2048; if not then the Rx_deskew_not_detected goes active. Rx_deskew_not_detected also goes active if CM(Rx) is not present and BED transitions to the ERROR state. Deskew detection is not a separate function, but a condition reported after the deskew process (the search for optimum sampling phase) has already been started.

[†] Rx_deskew_done is active if the BED completes the deskew process and the counter value is less than 2048; if not then the Rx_deskew_failed goes active. Rx_deskew_failed also goes active if CM(Rx) is not present and the BED transitions to the ERROR State.

5.3 Clock-data synchronization (Deskew)

5.3.1 Initialization deskew

During the initialization process and the DESKEW-1 STATE on both the FED and BED the devices attempt to align the sampling clock signal at its most reliable instant. The method for aligning is implementation-specific and is not discussed in this standard.

Note that the deskewing for the BED is much simpler than the deskewing for the FED because the clock edges and data edges on the front-end device must be pre-aligned to be $90^\circ \pm 22.5^\circ$ apart, see Figure 18. The Electrical Layer constraints on the line length differences between clock and data keep the deskewing on the BED relatively simple. The deskewing on the FED needs to be able to handle arbitrary but constant phase offset. It is recommended that the FED cover the full range of possible phase shifts from the round trip delay. In cases where the phase cannot be kept constant, an additional optional return clock can be implemented. The Tx data and the clock edges are aligned to be $90^\circ \pm 22.5^\circ$ apart in this case.

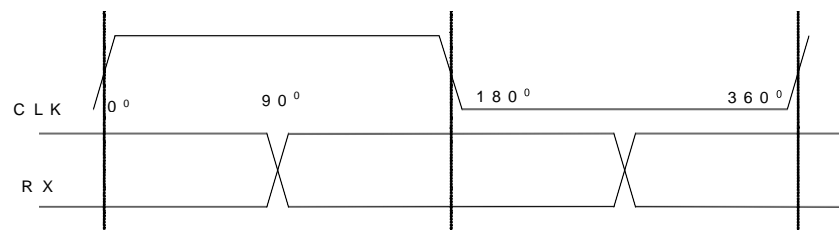


Figure 18 — Clock and data pre-alignment requirements

5.4 Sync mark

The sync mark is used to as a start of frame for the receiver to align with the transmitter's frame boundaries and precedes each frame. The pattern is **(0)1011** from first to last bit transmitted. A sequence matching circuit on the receive side of the interface scans for this pattern at the beginning of the frame. Once a sync has been detected, the decoding of the header bits along with the values in the frame format registers and frame boundary registers shall be used to compute the length of the frame. The sequence matching circuit must wait until the end of current frame as determined by the computed length of frame value before searching for the sync mark.

5.5 States of operation

There are three main states of operation for the link; LINK STATE, SLEEP STATE and Power-Off STATE. The LINK STATE is further sub-divided into a mandatory Continuous mode and an additional optional Duty-cycle mode.

5.5.1 Link STATE – Normal operation

In the LINK STATE the serial link is operational. Data, Control and Register bit information is transferred between the FED and the BED. When the FED and the BED are in their respective LINK STATES, the BED reads the capability registers of the FED and selects the frame parameters such as width of data word, number of data words in a frame, width of the control word, number of control words per frame and frame length multiple from the options supported in the FED by writing of the FED registers by the BED. Once the frame parameters are established control and data information can be exchanged. Refer to clause 7 for register definitions.

The LINK STATE is sub-divided into continuous mode and duty-cycled mode.

5.5.1.1 Link STATE - Continuous mode

During and immediately after initialization, the Link Layer shall use the Continuous Mode. In this mode, the Clock signal is kept active at all times. This clock can be used as the primary controller clock for the BED. Also, in this mode the data signals are kept at common mode on, even during the time when frames do not need to be communicated. The support for continuous mode is mandatory in the FED.

5.5.1 Link STATE – Normal operation (cont'd)

5.5.1.1 Link STATE – Continuous mode (cont'd)

In the continuous mode of operation, the transport layers on the BED and the FED has an option to monitor incoming parity errors (if the parity generation has been enabled). The threshold for when the detected occurrence of parity errors causes a transition to ERROR STATE is implementation specific. If the FED reaches its threshold of maximum allowable parity errors², it transitions from LINK STATE to ERROR STATE. In this state, the CM(Rx) is set to low, which causes the BED to transition from the LINK STATE to its ERROR STATE. The BED can also transition into its ERROR STATE if it reaches its maximum allowable parity errors. When the BED enters the ERROR STATE it can keep a count of the number of attempts to initialize before progressing to the START_INIT STATE to reestablish the link. The BED also sets CM(TX) to low or pulses the CM(TX)=low for less than 1us. If the number of attempts to establish the link exceed a max count threshold (implementation specific), the BED can transition to the SLEEP STATE and wait for a higher-level signal to re-start the initialization process. For example the BED state machine can be defined for 16 attempts to initialize before it turns itself off.

5.5.1.2 Link STATE - Duty-cycled mode

In the duty-cycled mode, the data and the clock can be duty-cycled to save power. This mode is an interface option and is sub-divided into duty cycle data and duty cycle clock sub-modes. The capability registers on the FED indicate support for either or both the sub-modes. The BED has the option of using either or both the sub-modes if these are supported on the FED.

In the duty-cycle modes, once the link has been established, on receipt of a Link_Request the Electrical Layer is required to raise the common mode transmit data voltage on the signaling pair. When a clock signal from the FED is active, the Transport Layer may start transmitting bits through the Link Layer beginning with a Sync Mark. This initial ramp is not part of the Sync Mark. Frames begin with the common mode rising. The Logic Level of the Data Common Mode during turn on is a zero (0). If the interface clock is not detected by the BED, the Link Layer on the BED reports a Link_Error to the Transport Layer. The detection period starts from raising of the common-mode transmit data voltage and is implementation specific.

5.5.1.2.1 Link STATE - Duty-cycled data sub-mode

In this sub-mode the data pins (Rx and Tx) can be duty cycled to save power. The state diagram transitions remain essentially the same except for the signaling of ERROR STATE transition between the FED and the BED. The ERROR STATE transition indication cannot be achieved by simply taking the common mode on the Rx and Tx pins low. To signal ERROR STATE transition in this sub-mode, the Rx and Tx pin common mode level must be pulsed off for less than 8 clock cycles, followed by a common-mode on for less than 8 clock cycles before it is set to off. As the minimum frame size will always be more than 8 clock cycles the frame transitions cannot be misinterpreted as a duty cycle event. This method of signaling is required for both the duty-cycled sub-modes shall not be used in the continuous mode of operation.

5.5.1.2.2 Link STATE - Duty-cycled clock sub-mode

In this sub-mode the clock signal along with the data pins (Rx and Tx) can also be duty cycled to save power. The state diagram transitions are similar to the duty-cycled data sub-mode. This option is useful only when the BED does not use the FED clock as a primary controller clock. When both sides are finished sending the current frame in progress the clock driver turns off after at-least M clock cycles as defined in clause 7. The clock can turn on based on the FED FIFO status. The FED checks the Rx_FIFO_Empty and RX_FIFO_Full Register. In heavy streaming, the Clock will automatically start when either the RX or TX streaming FIFO nears empty.

²INFORMATIVE: For example, either side can be programmed, via the device specific registers referenced in 7.1.4, to re-initialize the link if two parity errors are received during eight consecutive frames.

5.5.1.2 Link STATE - Duty-cycled mode (cont'd)

5.5.1.2.2 Link STATE - Duty-cycled clock sub-mode (cont'd)

However, the FIFO-triggered clock initiation is not the only way a Link may be requested. When the BED requests a Link, the common mode is raised on the Tx data line. The FED then initiates the clock and raises its common mode on detecting the common mode of the Tx line. When the clock and its common mode are detected on the BED, the Link Layer reports a Link_Ready to the Transport Layer.

5.5.2 Sleep STATE

In the Sleep STATE for both the FED and BED, the drivers are powered down and the clock and data common mode is low. The BED can place the FED in a SLEEP STATE by writing to the RESET register as defined in 7.1.1. The FED can also transition into SLEEP STATE from the RESET STATE after a time out period of 10 us for which the VCM(TX)=OFF.

The FED then shuts down its interface circuits (not necessarily the front-end device) including the interface clock source. The FED interface remains in this state until it detects a raised common mode from the BED. This is meant to awaken the FED and initialize the RESET mode register to an awakened state - RESET STATE. The difference between Duty-Cycled Clock Mode and SLEEP STATE is that in the SLEEP STATE the internal oscillator for the clock line is shut down. The wake up time requirements is the same as those from power up. Wake-up timing is at least long enough for the PLL to restart.

5.5.3 Power off STATE

When power is cut off from the device, the interface is in power off state. This is similar to SLEEP STATE except that the interface cannot wake up from power off until the power is restored to the device.

5.6 Slower speed, shorter distance and lower power

The electrical layer must operate in one of four power modes – which are distinguished by different transmission impedance levels. The high power mode utilizes a standard differential source and load termination impedance of 100 Ω . This mode enables data links with transmission rates up to 2.3 Gbps per data pair and up to a maximum distance of 50 cm at full rate.

The three low-power modes utilize higher transmission impedance to save driver power. These additional modes utilize nominal differential termination impedances of 200 Ω or 300 Ω , or high impedance, and are restricted for use with shorter interconnect distances and lower rates.

The power modes can be decided a priori between the FED and the BED and an optional impedance device mechanism is defined in which the power mode is set by the BED from the set of options defined in the capability registers on the FED. The BED can read these capability registers by register access. The capability registers are defined in clause 7. Both the FED and BED must power-up in a priori assigned mode. After device capability discovery the BED can program both the FED and BED to use one of the modes that both devices support. If power modes change, then the link must go through re-initialization and deskew.

5.7 Extensibility

This interface provides a path to needs of future WLAN interfaces. The interface data rates can be extended to higher bandwidths with lower latencies by using additional differential data lines. For applications requiring high data rates an additional differential lines (a RX and a TX) can be added. The additional data lines must be framed in accordance to the interface standard i.e. include the sync and header information. The data transfers over plural pairs in a single directional can only be enabled if both devices support a mutually acceptable number of pairs. The access of the FED and BED registers must continue to use the primary link.

5 Link layer (cont'd)

5.7 Extensibility (cont'd)

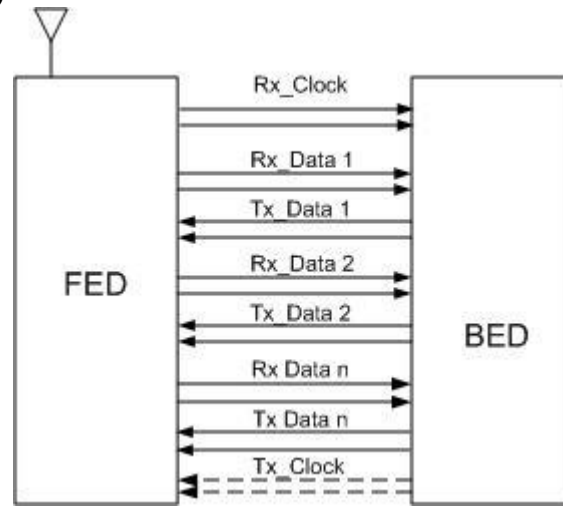


Figure 19 — Extensibility options

6 Transport layer

The Transport Layer provides communication of specific data types for example Samples, Control Bits, and Register Addresses. The Transport Layer provides access to registers that the BED may use to change Link Layer Power Modes and Electrical Layer Data Rates from the default settings. The programming of the registers does not change the clock frequency of the FED generated clock. The RF-BB frame is described as a sequence of fields in specific order. Figure 20 depicts the fields as they appear in the RF-BB frame and in the order in which they are passed between the FED and BED, from left to right. A sync mark is followed by a header field followed by frame type such as streaming data, control, register access or combination of the three.

The bit order and byte order is Little Endian. All bits within fields are numbered, from 0 to k, where the length of the field is k+1 bits. The bits are sent to between the FED/BED in order from the lowest numbered bit to the highest numbered bit. All bytes within a field are numbered, from 0 to K, where the number of bytes is K+1 bytes. The bytes in fields longer than a single byte are sent between the FED/BED in order from the lowest numbered byte to the highest numbered byte. Any group of sequential bits specified to contain a CRC value, but not any non-CRC bits that may be present in the same field, is an exception to this convention and is transmitted commencing with the coefficient of the highest-order term.

Reserved fields and subfields are set to 0 upon transmission and are ignored, other than for the purposes of computing parity and/or CRC check values, upon reception.



Figure 20 — General frame format

6 Transport layer (cont'd)

6.1 Transport service

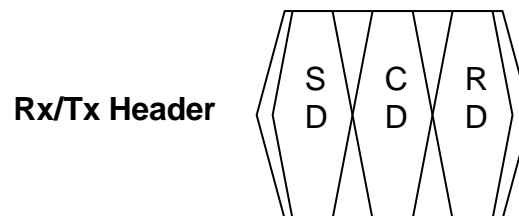
The transport layer transfers data to and from its local Core Logic and also transfers information to and from the Link Layer on either side of the interface. From Core Logic to Link Layer, the transport layer serializes and formats data and from Link Layer to the Core Logic, the transport layer de-formats and de-serializes the data.

Figure 12 illustrates the various components associated with the transport, link and electrical layers for the FED and BED. These general signal types are not necessarily comprehensive or sufficient, but are meant to be illustrative of the kinds of signals passed between the layers. These signals are defined in 3.1.

6.2 Initialization

Upon receiving the first Link Ready from the Link Layer, the BED will read the FED registers for capability information. From this and local information, the BED will determine the sizes of fields for streaming and control. During initialization the BED must use the continuous mode and after reading the capability registers on the FED, the BED can elect to use Duty-Cycled Clock and Duty-Cycled Data sub-modes and program the Mode Register, subject to the FED offering this capability.

6.3 Header field



Rx/Tx Header
SD: Streaming Data Bit
CD: Control Data Bit
RD: Register Data Bit

Figure 21 — Frame Header

Immediately following the Sync Mark is the Header field. The Header field shall be 3 bits in length, with the bit usage as shown in Figure 21. This field indicates to the receiver what type of frame payload and format to expect. The following bits are in transmit order:

- Streaming Data Bit
- Control Data Bit
- Register Data Bit

A “1” in each of these bits indicates the presence of streaming data, control data or register data within the frame. A “111” indicates the presence of all three fields (Streaming Data, Control Data and Register Data) while a “000” indicates no data; the other combinations indicate the various combinations of the fields.

6 Transport layer (cont'd)

6.4 Streaming data field

This field is intended to transfer data that updates very often and needs low latency thus accommodating multiple samples per frame. When the Streaming Data bit is set to 1, then the ensuing frame consists of streaming data which is followed by control and register information if indicated by the header. The number of data words per frame and the bit width of the data word is set by the BED from a set of options defined in the capability registers on the FED. The BED can read these capability registers by register access. The capability registers are defined in clause 7.

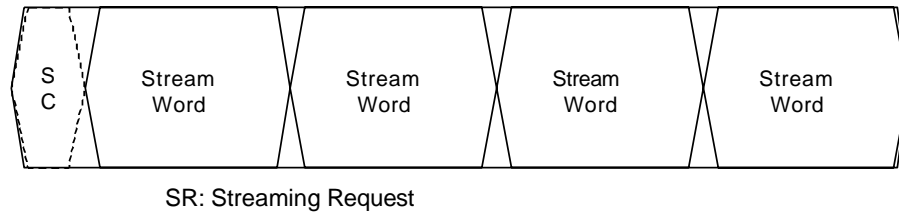


Figure 22 — Streaming field example

6.4.1 Stream Data

The streaming data field transports Number_Stream_Word data words, each of which contain Stream_Word_Length bits. The Streaming control Bits in the Mode register can be set to allow for dynamic streaming payload (see 6.4.2). The streaming data field transfers sample data or symbol data. In the case of sample data, it makes no distinction between back-end device I or Q data or IF-samples. In fact, I and Q pairs of data can be grouped into a single complex sample [I, Q]. For proper system operation both the FED and the BED are required to have a common understanding of the meaning of the streaming words, the transport layer does not need to know the meaning of the data it transfers.

The data frame width and data frame number registers define the Stream_Word_Length and the Number_Stream_Word per frame.

6.4.2 Streaming Control Bits (SC)

The Streaming Control (SC) bits are a streaming data option. The BED can select this option by programming the Mode register subject to this capability being indicated in the capability registers. When use of Streaming Control is enabled, receipt by the BED or FED of a Streaming Data field with SC=2'b01 is interpreted as a streaming data field has a dummy word inserted in it's last slot and SC=2'b10 is interpreted as a streaming data field has two dummy words inserted in the last 2 slots. The use of SC=2'b11 is reserved for future use.

| SC (MSB) | SC (LSB) | Condition |
|----------|----------|-------------------------------------------|
| 0 | 0 | No Dummy words inserted |
| 0 | 1 | Last word in the frame is a dummy word |
| 1 | 0 | Last 2 words in the frame are dummy words |
| 1 | 1 | Reserved |

These bits are useful when controlling the data rates. By offering the FED and BED a method to control the word rate per frame the interface does not constrain the user to using an interface clock that is a multiple of the sample clock.

The use of the SC bits is optional and is controlled by the SC_Use bit in the Mode Register. The SC bit is only present in the streaming data field (as indicated in Figure 22) when the SC_Use bit = 1. Clause 7 defines the register.

6 Transport layer (cont'd)

6.5 Control data field



Figure 23 — Control data frame

When the “Control data” bit in the header is set to ‘1’, the ensuing frame contains a control field. The frame can contain both streaming data and control information or simply one or the other. Figure 23 shows a frame consisting of the SYNC mark, followed by a header field, a streaming data field, 2 control words marked as CTL1 and CTL2 and a parity bit. Setting both the stream data bit and the control data bit to ‘1’ indicates that the frame will have both types of data simultaneously. The control field is intended to carry user defined WLAN IC control data such as AGC, Enables, Antenna Selection, etc.

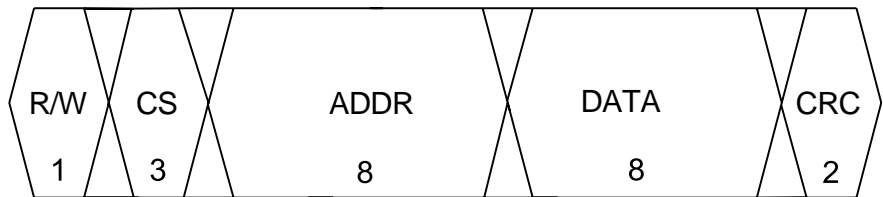
This field contains data that can change once per frame. The control field size and word lengths can be programmed using the parameters `Number_Control_Word`, and `Control_Word_Length` in the Control Format Registers.

Maximum control word length is 8 and the maximum number of `N_Control_Word` is 15. The control format registers define the control word length and the number of control words per frame.

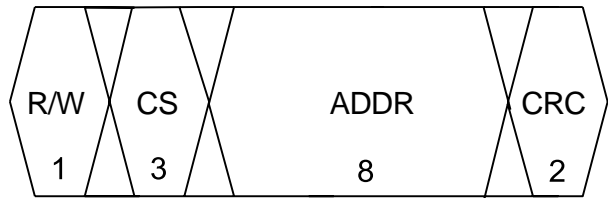
6 **Transport layer (cont'd)**

6.6 **Register data field (Configuration)**

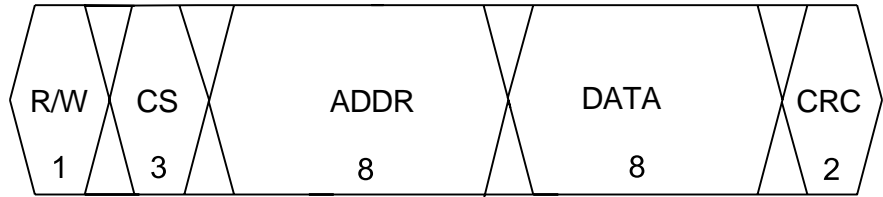
This field is intended to carry data for the configuration of the Link and Transport Layers of the RF-BB interface along with WLAN IC configuration data, 802.11 Signal and Length parameters, and lower-latency control data. Register Access also has the ability of programming sub-devices and/or co-integrated devices. The Tx-direction register data field has the following fields:



Register Write: BED to FED



Register Read: BED to FED



Register Read Response: BED to FED

R/W: Read/Write Bit (0: read, 1: write)
CS: Device/Chip Select Bits (2:0)
Address Sub-Field (8 bits)
Data Sub-Field (8 bits)
CRC Sub-Field (2 bits)

Figure 24 — Register data frames

The FED must respond to a read request within the next eight frames, failing which the BED has the option to either resend the request or transition into an error STATE. In the event that a link failure has occurred and FED does not respond with any frames; the BED shall wait for 1024 clock cycles for a read response. In the event that the register value is unavailable the FED can respond with the contents of a user defined status register.

The BED is allowed to send four read requests back to back while waiting for a read response. On sending a read request on a non-existing register the FED sends out a response with the data field filled with all zeros.

6 Transport layer (cont'd)

6.6 Register data field (Configuration) (cont'd)

The Chip Select bits are used to route to devices further down the chain of devices (pass through) or to devices sharing one end of an interface. For example a 2.4 GHz Front-end device and a 5 GHz front-end device may be on the same IC, share one interface to a common back-end device, but have their own sets of registers. The Chip Select bits can also be used to differentiate Registers for the interface and registers for the WLAN IC. A 3-bit space essentially allows for an eight-page register space to be implemented. The CS address 3b'000 must be used for the device on which the interface resides. The use of other bit addresses is implementation specific, for example 3'b001 can indicate the register page for a 5GHz radio.

A random set of errors on the link can program the FED into an unknown state. To ensure that the registers are programmed correctly, a 2-bit CRC checksum is implemented on the register field. The CRC must be checked and validated for read requests, read responses and before a register is actually written. A 2-bit CRC will offer 100% detection of a 2-bit burst error, 87.5% detection for a 3b error and a 75% error detection probability for errors greater than 4 bits. The polynomial $g(x) = x^2 + x + 1$ shall be used. The CRC checksum is sent out as "Big Endian" unlike the rest of the transport layer bit order.

A CRC failure is indicated in the exception register, referred in clause 7. When a CRC failure is detected on the FED during a write or read command from the BED, the FED ignores the write command and responds back with the value in the status register with the CRC bit set as "1" along with its register address. When a CRC failure is detected on the BED during a read response from the FED, the BED has the option to re-send the read command or re-initialize the serial link. The decision to re-initialize is implementation specific.

6.7 Parity (P) field

The parity check on the FED and the BED is turned off in the default state. The BED can request the parity check and parity field generation to be turned on by setting the Use Parity bit in the Mode register, subject to having this capability available on the FED. The interface uses the parity field at the end of the frame in the case that the Use Parity bit = 1. The Parity field contains one bit and maintains an even number of logical 1s in the frame not counting sync mark but includes the header field, and rest of the data fields.

The handling of parity error is implementation specific.

6.8 Frame boundary and null field

A minimum frame multiple variable "M" is defined to simplify implementations. The total bit interval between sync + header and the next sync + header shall be a multiple "M". The minimum frame variable must be even so that the frame lasts an integer number of clock cycles. This does not constrain the payload to be of a fixed length but may require a null field before the next sync. A null field is defined as integer number of bit periods of no data and the differential data pins are set to a logical "0". This constraint applies only to the continuous mode. In the duty-cycle mode the clock will cease after the transfer and the data pins will be held at common-mode off, hence not requiring the null field.

For example if M=12; and the payload (a data, control or register sub frame) is b'138b, then at least b'6 of Null must be sent out before the next sync. This example calculation is for illustration only and the frame length can be of any value. The Null Bits are set to 0's so that the parity checker is unaffected by these Null bits. The location of the parity bit is required to be at the end of frame and before the null bits.

7 Registers

The RF-BB interface standard requires a number of registers in the front-end device to configure and control the interface. Registers in the front-end device defining the functionality of the front-end device itself are out of the scope of this specification and are being considered by the “Interoperability and Compliance” task group.

7.1 Register overview

Registers are located in the front-end device. The back-end device is assumed to have knowledge of the front-end device’s programming model and may keep a local copy of the FED’s registers. The address space from 00h to 1Fh is reserved for interface specific registers. The remaining register addresses are available for implementation specific registers. The “Interoperability and Compliance” task group is working on standardizing part of the implementation space for future versions of the RF-BB standard.

The Interface registers are further sub-divided into a set of mode selection and status registers, capability read-only registers and personality read-only registers. The mode selection registers when programmed by the BED control the modes of the interface based on the status it reads out. The capability registers indicate the FED’s interface capability such as frame formats, data width, number of data words per frame, and control frame format. The personality registers list the manufacturer’s identification number, the FED device number and the version number of the standard supported.

7.1.1 Interface registers

RESET REGISTER

| Add | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|-----|-------|----------|----------|----------|------------|-------------|-------------|-------------|-----------|-----|-----|
| 00 | RESET | Reserved | Reserved | Reserved | POWER DOWN | ERROR STATE | SLEEP STATE | RESET STATE | RESET REG | 00 | R/W |

RESET REG: Setting the bit high will reset the registers on the FED to their default values. The reset register will also be reset to “0”.

RESET STATE: When high the FED Interface will be put into the RESET STATE; in this mode, the Clock is off and RX common mode is held active.

SLEEP STATE: Setting the bit high will put the FED Interface into the SLEEP STATE; in this mode the Clock is OFF and the RX is common mode low.

ERROR STATE: Setting the bit high will force the FED Interface to go into Error State

POWER DOWN: Setting the bit high will power down the FED including the internal PLL. The interface will transition into SLEEP Mode. The registers will be reset to default state. A common mode active detection on the Tx pin will transition the FED out of this mode.

With the exception of the RESET REG when any of the other bits in the RESET Register are set, the link becomes non-operational and needs to be re-initialized based on the initialization state machine and the reset register values go to their default states.

MODE REGISTER

| Add | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|-----|------|----------|-----|-----|------------|--------|-----|-----|----------|-----|-----|
| 01 | MODE | Reserved | PM1 | PM0 | USE PARITY | USE SC | DCC | DCD | Reserved | 01 | R/W |

DCD: When high the FED is in the duty cycle data mode; this mode is enabled only if the FED capability registers indicate support for this mode and the CM bit is set to “0”.

DCC: When high the FED is in the duty cycle clock mode; this mode is enabled only if the FED capability registers indicate support for this mode and the CM bit is set to “0”

7.1 Register overview (cont'd)

7.1.1 Interface registers (cont'd)

| DCC | DCD | Mode | Support |
|-----|-----|---------------------------|-----------|
| 0 | 0 | Continuous Mode | Mandatory |
| 0 | 1 | Data Duty Cycle Sub-Mode | Optional |
| 1 | 0 | Clock Duty Cycle Sub-Mode | Optional |
| 1 | 1 | Clock Duty Cycle Sub-Mode | Optional |

USE SC: When high, the SC (Streaming control bits) are present in the streaming data field; this mode is enabled only if the FED capability bit indicates capability.

USE PARITY: When high the command will enable the generation and checking of parity on the FED; this mode is enabled only if the FED capability registers indicate support for this mode

PM1, PM0: Power Mode registers. Programming these registers puts the interface in different power modes. These modes can be enabled only if the FED capability registers indicate support for this mode. On changing power modes the FED the link becomes non-operational and needs to be re-initialized based on the initialization state machine.

| PM1 | PM0 | Mode | Support |
|-----|-----|------------------|-----------|
| 0 | 0 | High Power Mode | Mandatory |
| 0 | 1 | Low Power Mode 1 | Optional |
| 1 | 0 | Low Power Mode 2 | Optional |
| 1 | 1 | Low Power Mode 3 | Optional |

FIFO STATUS REGISTER

| Add | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|-----|---------|----------|----------|----------|----------|-----------------|------------------|-----------------|------------------|-----|-----|
| 02 | FIFO_SR | Reserved | Reserved | Reserved | Reserved | RX_FIF O_EMP | RX_FIF O_FULL | TX_FIF O_EMP | TX_FIF O_FULL | 00 | R |

TX_FIFO_FULL: A high indicates that the TX_FIFO on the FED is close to its capacity

TX_FIFO_EMPTY: A high indicates that the TX_FIFO on the FED is low on data

RX_FIFO_FULL: A high indicates that the RX_FIFO on the FED is close to its capacity

RX_FIFO_EMPTY: A high indicates that the RX_FIFO on the FED is low on data

EXCEPTION REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|-----|-----------|--------|-------------|-------------|-------------|---------------|---------------|------------------|------------------|-----|-----|
| 03 | Exception | Extend | TEMP (2) | TEMP (1) | TEMP (0) | PLL Status | CRC Status | Parity Status | DeSkew Status | 00 | R |

The implementations of register are mandatory, but reporting status is optional.

Deskew Status: A high indicates a deskew error; Criteria for deskew error is implementation specific.

Parity Status: A high indicates an occurrence of parity error; the error status remains valid until the exception register value is sent back to the BED

CRC Status: A high indicates a CRC error during the last frame; if an error is indicated the FED will send the value of the status register back to the BED autonomously. This will reset the CRC bit.

PLL Status: A high indicates that the PLL is unlocked.

TEMP(2:0): The coding of temperature is as follows – A 3'b000 indicates that the feature is not supported and a b'001-b'111 are increasing values, while leaving the specific interpretation of the non-zero codes to the implementer of the FED.

Extend: A high indicates that an extended status is available at an implementation specific address.

7.1 Register overview (cont'd)

7.1.1 Interface registers (cont'd)

FORMAT USE REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|-----------|--------|-----|-----|----|----|-----|-----|-----|-----|-----|-----|
| 04 | Format | PLM | PLM | CF | CF | DF2 | DF2 | DF1 | DF1 | 03 | R/W |

DF1: Selects the Stream_Word_Length value from one out of four registers. (00-Addr 06'h; 01-Addr 07'h; 10-Addr 08'h; 11-Addr 09'h)

DF2: Selects the Number_Stream_Word value from one out of four registers. (00-Addr 0A'h; 01-Addr 0B'h; 10-Addr 0C'h; 11-Addr 0D'h)

CF: Selects the control field format value from one out of four registers pairs. (00-Addr 0E'h, 12'h; 01-Addr 0F'h, 13'h; 10-Addr 10'h, 14'h; 11-Addr 11'h, 15'h)

PLM: Selects the Frame length multiple value from one out of four registers. (00-Addr 16'h; 01-Addr 17'h; 10-Addr 18'h; 11-Addr 19'h)

7.1.2 Capability registers

FORMAT CAPABILITY REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|-----------|--------|-----|-----|-----|--------|----|-----|-----|----------|-----|-----|
| 05 | FORMAT | LP3 | LP2 | LP1 | PARITY | SR | DCC | DCD | Reserved | 00 | R |

DCD: A high indicates that the FED is capable of supporting Duty Cycle Data Mode.

DCC: A high indicates that the FED is capable of supporting Duty Cycle Clock Mode and Duty Cycle Data Mode

SC: A high indicates that the FED is capable of supporting the Streaming Request Bit in the Streaming Data Field.

PARITY: A high indicates the FED is capable of supporting parity generation and parity check

LP1: A high indicates the FED is capable of supporting the low power mode 1

LP2: A high indicates the FED is capable of supporting the low power mode 2

LP3: A high indicates the FED is capable of supporting the low power mode 3

DATA FRAME WIDTH REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|--------------|------------------|------|----------|----------|----------|-----|-----|-----|-----|-----|-----|
| 06-09 | Data Frame Width | SWLX | Reserved | Reserved | Reserved | SWL | SWL | SWL | SWL | 00 | R |

This is a set of 4 registers with identical formats.

SWL: Indicates the Streaming_Word_Length. The number of streaming word length in each frame is SWL+1. Four options can be made available by the FED to accommodate different types of length streaming data words. The Streaming_Word_Length is selected by the BED by programming the FORMAT USE REGISTER.

SWLX: A high indicates that the FED supports a custom streaming word length that is defined in an implementation specific register. The extension bit is provided for applications that require streaming word lengths that are greater than 16.

7.1 Register overview (cont'd)

7.1.2 Capability registers (cont'd)

DATA FRAME NUMBER REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|--------------|-------------------|------|----------|----------|----------|-----|-----|-----|-----|-----|-----|
| 0A-0D | Data Frame Number | NSWX | Reserved | Reserved | Reserved | NSW | NSW | NSW | NSW | 00 | R |

This is a set of 4 registers with identical formats.

NSW: Indicates the Number_Stream_Word per frame. The number of stream words per frame is NSW+1. The Four options can be made available by the FED to accommodate different types of number of streaming words. The Number_Stream_Word per frame is selected by the BED by programming the FORMAT USE REGISTER.

NSWX: A high indicates that the FED supports a custom number of streaming words per frame that is defined in an implementation specific register. The extension bit is provided for applications that require number of streaming words to be greater than 16.

CONTROL FRAME WIDTH REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|--------------|-------------------------|------|----------|----------|----------|----------|-----|-----|-----|-----|-----|
| 0E-11 | Control Format Register | CWLX | Reserved | Reserved | Reserved | Reserved | CWL | CWL | CWL | 00 | R |

This is a set of 4 registers with identical formats

CWL: Indicates number of bits per control word. The number of bits per control word is CWL+1. Four options can be made available by the FED to accommodate different types of frame formats. The control field format is selected by the BED by programming the FORMAT USE REGISTER.

CWLX: A high indicates that the FED supports a custom word length that is defined in an implementation specific register. The extension bit is provided for applications that require the control word lengths greater than 8.

CONTROL FRAME NUMBER REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|--------------|-------------------------|------|----------|----------|----------|----------|-----|-----|-----|-----|-----|
| 12-15 | Control Format Register | NCWX | Reserved | Reserved | Reserved | Reserved | NCW | NCW | NCW | 00 | R |

This is a set of 4 registers with identical formats

NCW: Indicates the number of control words per frame when the header has control data available bit set high. The number of control words is NCW+1. Four options can be made available by the FED to accommodate different number of control words. The control field format is selected by the BED by programming the FORMAT USE REGISTER.

NCWX: A high indicates that the FED supports a custom number of control words per frame that is defined in an implementation specific register. The extension bit is provided for applications that require number of control words to be greater than 8.

7.1 Register overview (cont'd)

7.1.2 Capability registers (cont'd)

FRAME BOUNDARY REGISTER

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|--------------|-------------------------|----|----------|----------|----------|----|----|----|----|-----|-----|
| 16-19 | Frame Boundary Register | MX | Reserved | Reserved | Reserved | M | M | M | M | 00 | R |

This is a set of 4 registers with identical formats.

M: The total number of bits between sync mark followed by header and the next sync mark and header combination is an even integer multiple. The total number of bits is equal to $2*(M+1)$ where M is an integer ranging from 0 to 15. This does not constrain the payload to be of a fixed length but requires a null-field before the next sync. This constraint applies only to the continuous clock mode. In duty-cycle mode the clock will cease after the transfer and does not require the null-field. When the value of M is not known a priori, the initial register packets are transferred at M=15.

MX: A high indicates that the FED supports a custom frame boundary that is defined in an implantation specific register. The extension bit is provided for applications that require a frame boundary value greater than 16.

Four options can be provided to accommodate different frames boundaries. These are selectable by the format use register.

7.1.3 Personality registers

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Def | R/W |
|-----------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1A | MFG ID | MID | MID | MID | MID | MID | MID | MID | MID | | R |
| 1B | | MID | MID | MID | MID | MID | MID | MID | MID | | R |
| 1C | Device Type | DT | DT | DT | DT | DT | DT | DT | DT | | R |
| 1D | | DT | DT | DT | DT | DT | DT | DT | DT | | R |
| 1E | JC-61 Version | VER | VER | VER | VER | VER | VER | VER | VER | | R |
| 1F | | VER | VER | VER | VER | VER | VER | VER | VER | | R |

MFG ID: This is a 16-bit value, derived from the manufacturer's JEDEC-assigned ID code listed in JEP 106 for the purpose of uniquely identifying the manufacturers of JC-61 conformant devices. The low-order 8 bits of this value are read from register 1A and the high-order 8 bits are read from register 1B. Register 1A contains the last 8 bits of the manufacturer's ID value as listed in JEP106. Register 1B contains the number of continuation fields that appear at the beginning of the manufacturer's ID value as listed in JEP106.

EXAMPLE Analog Devices is represented by - Addr 1A → E5; Addr 1B → 01; RFMD is represented by – Addr 1A AE; Addr 1B → 03; Nvidia is represented by – Addr 1A → 6B; Addr 1B → 04;

Device Type: This is a 16-bit value, assigned by the manufacturer identified in the MFG ID of this device, for the purpose of uniquely identifying the type of this device among the full set of all types of FEDs, Lower MAC devices, and Upper MAC devices produced by that manufacturer. The low-order 8 bits of this device type value are read from register 1C and the high-order 8 bits are read from register 1D. It is strongly recommended that manufacturers assign a new Device Type value not only to identify new types of devices, but also to distinguish between major revisions that alter the functionality and/or characteristics of a preexisting device.

JC-61 Version: This is a pair of 8-bit values that identify the range of JC-61 versions supported by the device. The value in register 1E indicates the minimum supported version and the value in register 1F indicates the maximum supported version. The numbers that identify each version are specified in the appropriate JC-61 documents. Values in the range 00-7F are reserved for versions of the RF-BB interface, with the initial version being 00.

7.1 Register overview (cont'd)

7.1.4 Device specific registers

The RF-BB interface standard requires a number of registers in the front-end device to configure and control the interface. Registers in the front-end device defining the functionality of the front-end device itself shall use register addresses in the range of 20-FF. The format and functions of these registers are outside of the scope of this specification and are being considered by the “Interoperability and Compliance” task group.

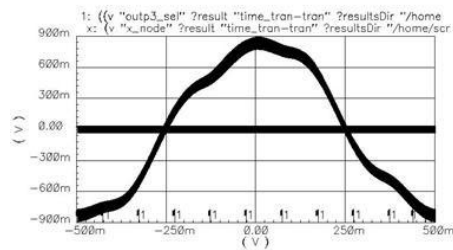
[illegible]

Annex A - Simulations

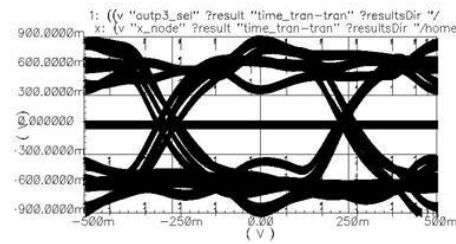
Case 1: Typical case

Zline=50Ω, 50cm Line loss=1.2dB@1.15GHz, CL=2.0pF, RL=50 Ω x 2, CDRV=1.8pF, LPKG=4nH

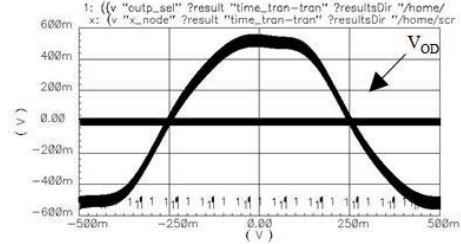
1150MHz Clock at transmitter end, edge rate= 8.2V/ns



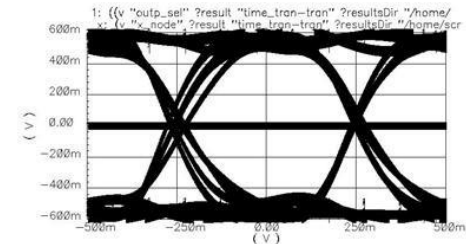
Data at transmitter end



1150MHz Clock at receiver end, edge rate= 4.4V/ns



Data at receiver end

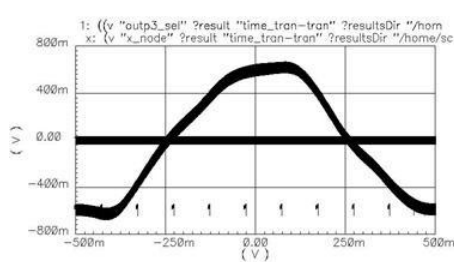


Data pattern: 00000,10110,01111,10100,01010,10101

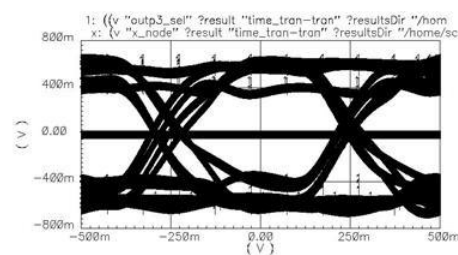
Case 1: Worst case

Rdriver+10%, Vsup-10%, slow, 125°C, Zline1,2=55,56.1ohm, line_delta=3mm(15ps), RL-10%

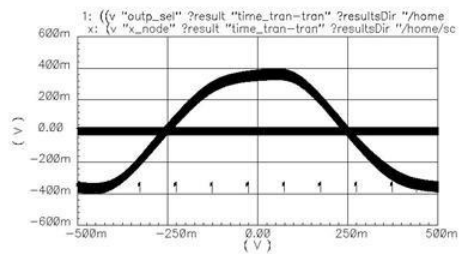
1150MHz Clock at transmitter end, edge rate= 4.6V/ns



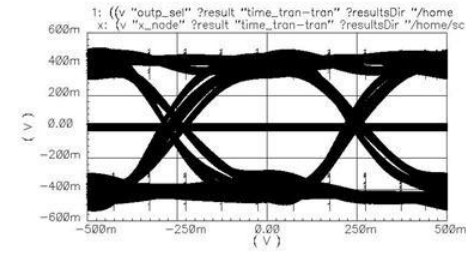
Data at transmitter end



1150MHz Clock at receiver end, edge rate= 2.9V/ns



Data at receiver end



Data pattern: 00000,10110,01111,10100,01010,10101

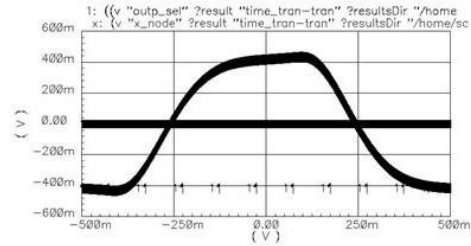
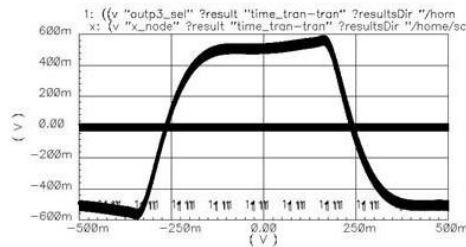
Annex A - Simulations (cont'd)

Case 2: Typical case

Zline=50 Ω , 100cm Line loss=1.5dB@600MHz, CL=4pF, RL=50 Ω x 2, CDRV=3pF, LPKG=4nH

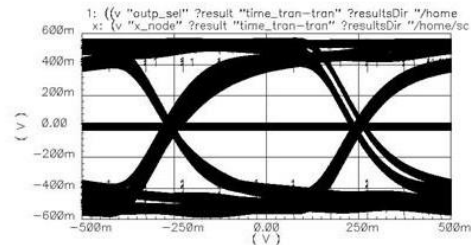
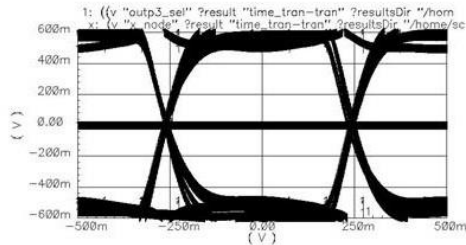
600MHz Clock at transmitter end, edge rate=4.7V/ns

600MHz Clock at receiver end, edge rate=2.4V/ns



Data at transmitter end

Data at receiver end



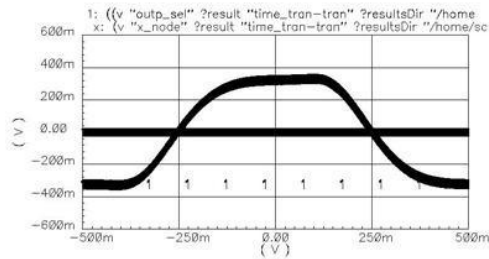
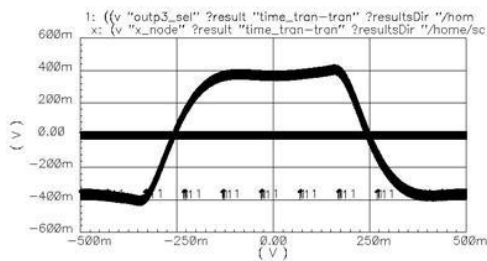
Data pattern: 00000,10110,01111,10100,01010,10101

Case 2: Worst case

Rdriver+10%, Vsup-10%, slow, 125°C, Zline1,2=55,56.1ohm, line_delta=6mm(30ps), RL-10%

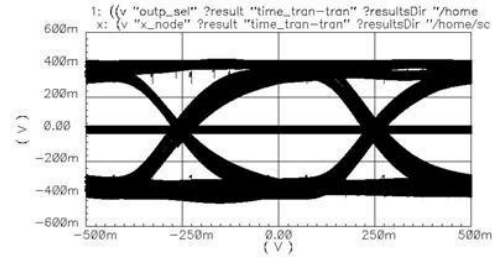
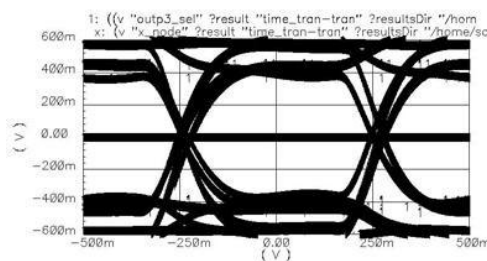
600MHz Clock at transmitter end, edge rate=3.3V/ns

600MHz Clock at receiver end, edge rate=1.9V/ns



Data at transmitter end

Data at receiver end



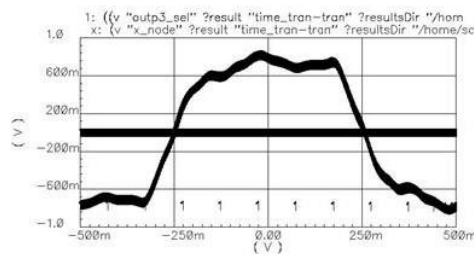
Data pattern: 00000,10110,01111,10100,01010,10101

Annex A - Simulations (cont'd)

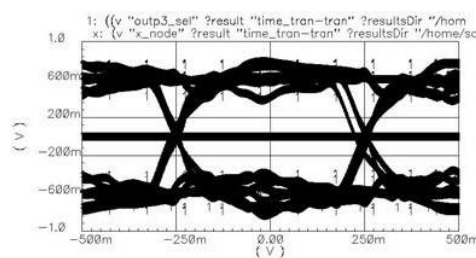
Case 3: Typical case

Zline=100Ω, 10cm Line loss=0.3dB@600MHz, CL=2pF, RL=100 Ω x 2, CDRV=1.8pF, LPKG=4nH

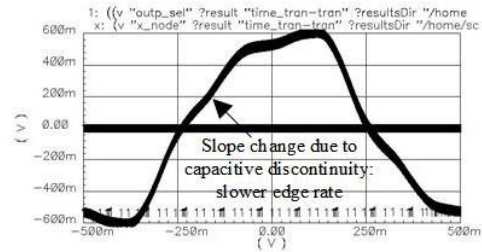
600MHz Clock at transmitter end, edge rate= 6.7V/ns



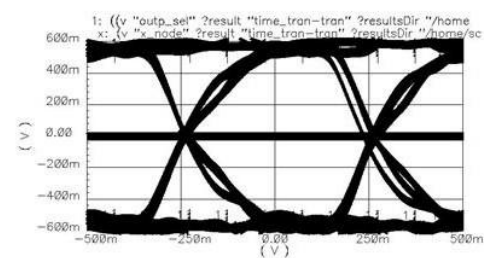
Data at transmitter end



600MHz Clock at receiver end, edge rate= 2.1V/ns



Data at receiver end

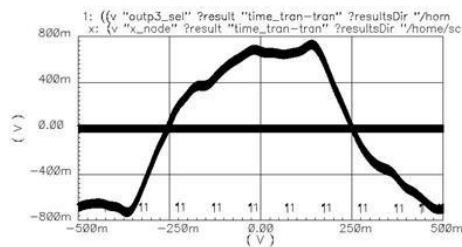


Data pattern: 00000,10110,01111,10100,01010,10101

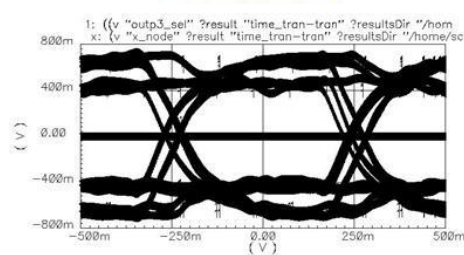
Case 3: Worst case

Rdriver+10%, Vsup-10%, slow, 125°C, Zline1,2=120,126ohm, line_delta=6mm(30ps), RL-10%

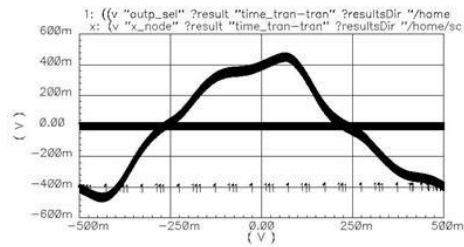
600MHz Clock at transmitter end, edge rate= 4.2V/ns



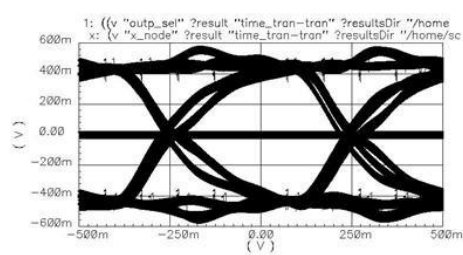
Data at transmitter end



600MHz Clock at receiver end, edge rate= 1.3V/ns



Data at receiver end



Data pattern: 00000,10110,01111,10100,01010,10101

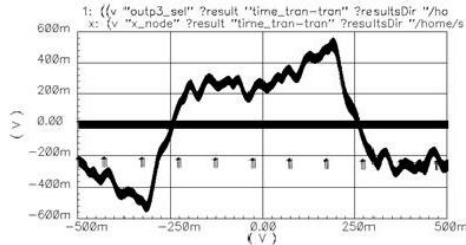
Annex A - Simulations (cont'd)

Case 4: Typical case

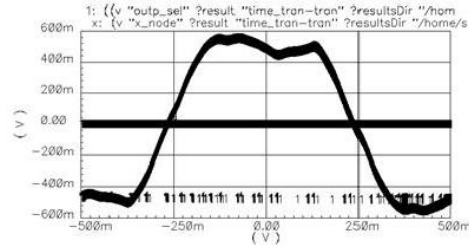
$Z_{line}=130\Omega$, 3 cm Line, $CL=2pF$, $RL=150\Omega \times 2$, $CDRV=1.8pF$, $LPG=4nH$

400MHz Clock at transmitter end, edge rate= 2.4V/ns

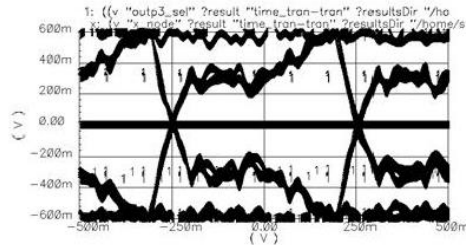
400MHz Clock at receiver end, edge rate= 2.1V/ns



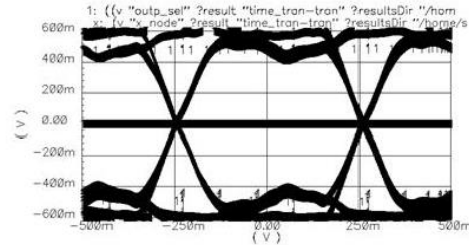
Data at transmitter end



Data at receiver end



Data pattern: 00000,10110,01111,10100,01010,10101

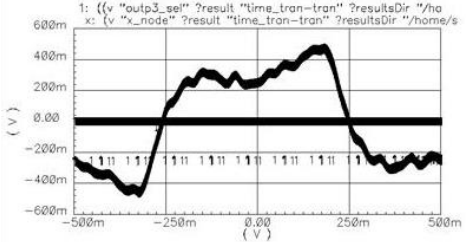


Case 4: Worst case

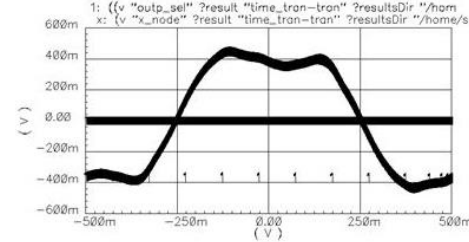
$R_{driver}+10\%$, $V_{sup}-10\%$, slow, $125^{\circ}C$, $Z_{line1,2}=150,157\Omega$, $line_delta=10mm(50ps)$, $RL-10\%$

400MHz Clock at transmitter end, edge rate= 2.1V/ns

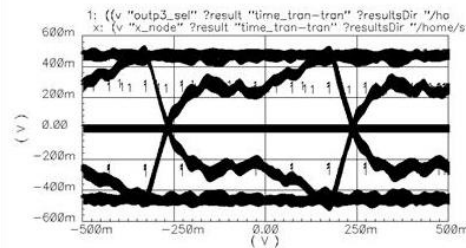
400MHz Clock at receiver end, edge rate= 1.9V/ns



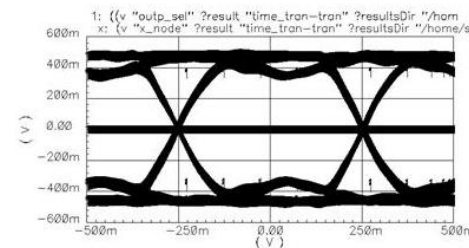
Data at transmitter end



Data at receiver end



Data pattern: 00000,10110,01111,10100,01010,10101

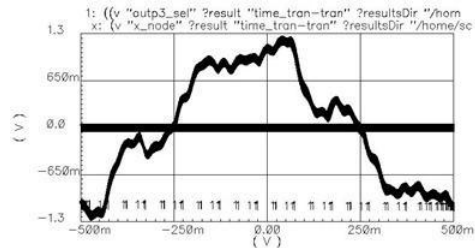


Annex A - Simulations (cont'd)

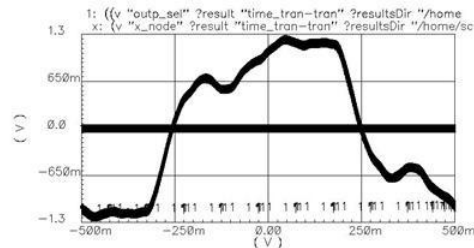
Case 5: Typical case

Zline=50 Ω , 5cm Line, CL=4pF, RL=10k Ω x 2, CDRV=3pF, LPKG=4nH

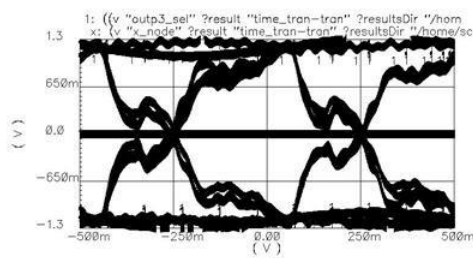
200MHz Clock at transmitter end, edge rate= 1.6V/ns



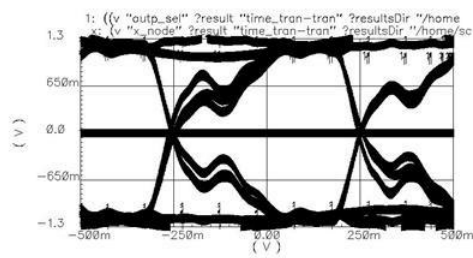
200MHz Clock at receiver end, edge rate= 3.3V/ns



Data at transmitter end



Data at receiver end

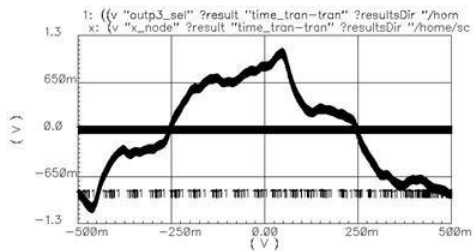


Data pattern: 00000,10110,01111,10100,01010,10101

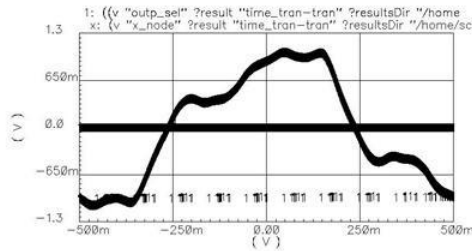
Case 5: Worst case

Rdriver+10%, Vsup-10%, slow, 125°C, Zline1,2=60,63 ohm, line_delta=10mm(50ps), RL-10%

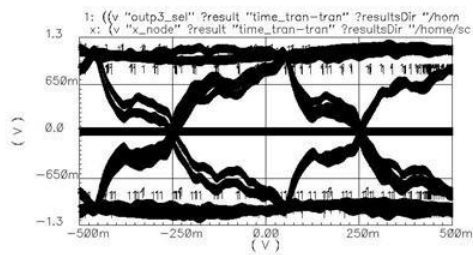
200MHz Clock at transmitter end, edge rate= 2.5V/ns



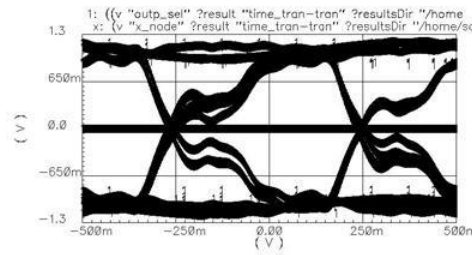
200MHz Clock at receiver end, edge rate= 2.1V/ns



Data at transmitter end



Data at receiver end



Data pattern: 00000,10110,01111,10100,01010,10101

Annex B – Clock frequency choice

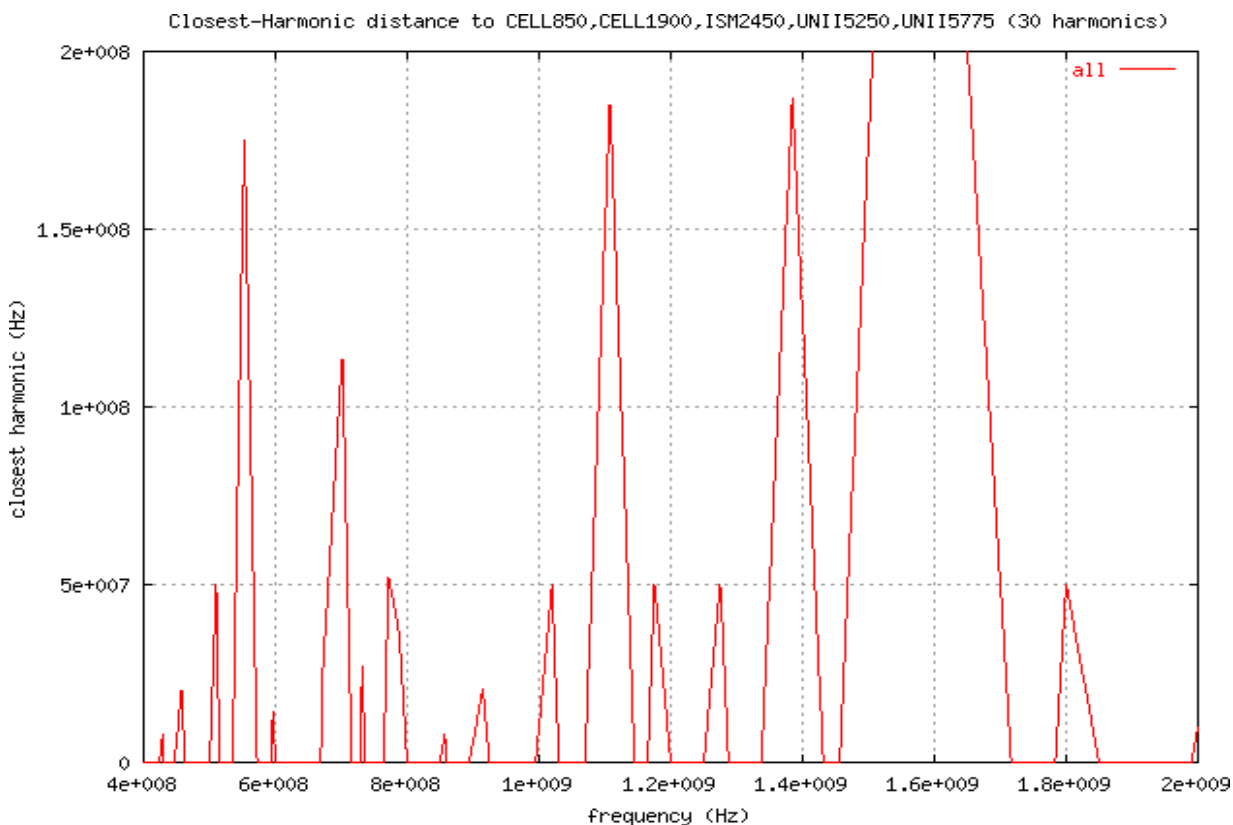


Figure B.1 — Closest harmonic distance from bands of interest.

B.1 Example

Consider the frequency 1.1 GHz and its 30 harmonics. These are 1.1, 2.2, 3.3, ..., 33 GHz. How close do any of these harmonics come to the CELL850, CELL 1900, ISM2450, or UNII bands? 1.1 GHz is 206 MHz from the top of the CELL850 band (894 MHz). The second harmonic at 2.2 GHz is 210 MHz away from the top of the CELL1900 band (1990 MHz). It is also only 200 MHz away from the bottom of the ISM band (2400 MHz). The fifth harmonic at 5.5 GHz is 150 MHz from the top of the Lower UNII band edge (5.35 GHz) and 225 MHz away from the bottom of the Middle/High UNII band edge (5.725 GHz). The Sixth harmonic, 6.6 GHz, is 775 MHz away from the top of the Middle/High UNII band edge (5.825 GHz). Thus, the closest any of these harmonics gets to any of the bands of interest is 150 MHz that is shown in the figure B.1.

Annex B – Clock frequency choice (cont'd)

B.2 Matlab/Octave Source

```
% ISMUNIISCAN.M
% Chuck Hwang
% (c) 2002 Channel Technology
% Octave/Matlab Script to evaluate Digital interface harmonics
% between 800 MHz and 1600 MHz in the ISM and UNII Bands

% Parameters
SCAN_START = 400e6; % Hz
SCAN_END = 2000e6; % Hz
SCAN_STEP = 0.5e6; % Hz
SCAN_ARRAY = SCAN_START:SCAN_STEP:SCAN_END;
SCAN_LENGTH = length(SCAN_ARRAY);
CLOCK_TOLERANCE = 1e-6;
PROXIMITY_TOLERANCE = 50e6; % Hz
N_HARMONICS = 30;

% describe bandlimits here
%[GSM850TX,GSM850RX,GSM1900TX,GSM1900RX,ISM,UNII_LOMID,UNII_HI]
LO_LIM = [824e6,869e6,1850e6,1930e6,2400e6,5150e6,5725e6];
HI_LIM = [849e6,894e6,1910e6,1990e6,2500e6,5350e6,5825e6];
N_BANDS=length(LO_LIM);
band_lim_string=["CELL850,CELL1900,ISM2450,UNII5250,UNII5775"];

%LO_ISM = 2400e6; %Hz
%HI_ISM = 2500e6; %Hz

%LO_LOMIDUNII = 5150e6;
%HI_LOMIDUNII = 5350e6;

%LO_HIUNII = 5725e6;
%HI_HIUNII = 5825e6;

% Loop-Scan the possible interface clock speeds
for scanindex = 1:SCAN_LENGTH,
    clockspeed=SCAN_ARRAY(scanindex);

    % Initialize Clock and Proximity Metrics

    % Loop-Scan N-th Harmonic of candidate clock speed
    for harmonic = 1:N_HARMONICS,
        harmonicspeed = harmonic*clockspeed;
        loharmonic = harmonicspeed*(1-CLOCK_TOLERANCE);
        hiharmonic = harmonicspeed*(1+CLOCK_TOLERANCE);

        % iterate through bands of interest
        for band=1:N_BANDS,

            % Test this band
            if ( ((LO_LIM(band)<loharmonic)&(loharmonic<HI_LIM(band))) | ...
                ((LO_LIM(band)<hiharmonic)&(hiharmonic<HI_LIM(band))) )
                harmproximity(band,harmonic)=0;
            else,
                harmproximity(band,harmonic) = min(abs([loharmonic-LO_LIM(band), ...
                                                            loharmonic-HI_LIM(band), ...
                                                            hiharmonic-LO_LIM(band), ...
                                                            hiharmonic-HI_LIM(band)]));
            endif
        end
    end
end
```

```
        endfor

        endfor
        proximity(scanindex)=min(min(harmproximity));
        % Collect band proximities
        allproximity(scanindex)=proximity(scanindex);
    endfor

    clg
    axis([SCAN_START,SCAN_END,0,4*PROXIMITY_TOLERANCE])
    grid("on")
    xlabel("frequency (Hz)")
    ylabel("closest harmonic (Hz)")
    title(["Closest-Harmonic distance to ", band_lim_string, " (",num2str(N_HARMONICS)," harmonics)"])
    plot(SCAN_ARRAY,allproximity,"-;all;")
```

Annex C (Informative) Differences between JESD96A.01 and its Predecessors

This Annex briefly describes the principal changes made to entries that appear in this standard, JESD96A.01, compared to its predecessors, JESD96A (February 2006) and JESD96 (April 2004). If the change to a concept involves any words added or deleted, it is included. Some punctuation changes are not included.

Differences between JESD96A.01 and JESD96A:

| Clause | Description of Change |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| General | Editorial revision that changes sensitive terminology (specifically, for two clauses) Updated JEDEC logo, cover pages and back pages to standard format. |
| 5.5.1.1 | Sensitive terminology replaced with “ primary controller ” clock... |
| 5.5.1.2.2 | Sensitive terminology replaced with “ primary controller ” clock... |

Differences between JESD96A and JESD96:

NOTE The main change is the addition of an optional return clock with the data and clock offset in phase by 90 degrees.

| Page | Description of Change |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| iii | Added: An optional pair of pins can be assigned for a return clock from the BED to the FED. |
| 1 | Added to Figure 1: Tx_Clock (dashed lines) |
| 5 | Added: An optional pair of pins can be assigned for a return clock from the BED to the FED. |
| 6 | Added to Figure 2: CLK and CLKN (dashed lines) |
| 16 | Added Section 4.7.1.2 Phasing of clock and Tx data outputs: In the case of the usage of the optional return clock , the clock and data outputs from the BED shall be nominally phased so that the clock edges and data edges are aligned to be 90° +/- 22.5° apart. |
| 23 | Changed on Line 3: common changed to differential Changed on Line 9: high to active |
| 24 | Added: The deskew process does not have to take the 2048 clock cycles and can complete earlier, and using an internal clock or if available the return clock from the BED. |
| 25 | Added: It can also be completed in shorter time than the maximum allowed. |
| 29 | Added: In cases where the phase cannot be kept constant, an additional optional return clock can be implemented. The Tx data and the clock edges are aligned to be 90° +/- 22.5° apart in this case. |
| 32 | Added to Figure 19: Optional Tx Clock (two dashed lines) |
| 40 | Added for CE: pairs Changed for PLM: 00-Addr 0E'h, 12'h; 01-Addr 0F'h, 13'h; 10-Addr 10'h, 14'h; 11-Addr 11'h, 15'h) to (00-Addr 16'h; 01-Addr 17'h; 10-Addr 18'h; 11-Addr 19'h) |

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Standard Improvement Form

JEDEC JESD96A.01

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

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The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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